SpaceWire AHB-Lite DMA IP Core

The SpaceWire AHB-Lite Interface IP core is a generic synthesisable VHDL model which can be instantiated in an AHB-Lite compatible system to move packet data between a SpaceWire network and system memory. SpaceWire is a data-handling network for use on-board spacecraft, which connects together instruments, mass-memory, processors, downlink telemetry, and other on-board sub-systems.

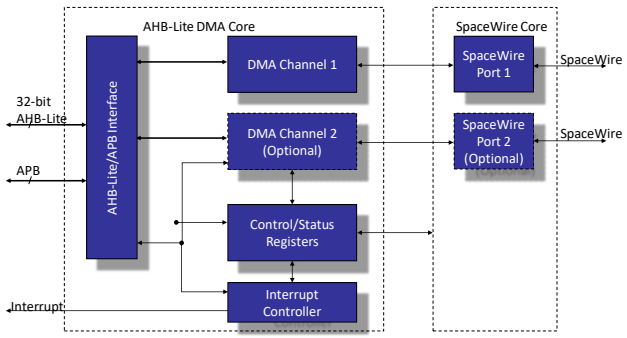
The core provides either 1 or 2 bi-directional DMA channels with SpaceWire interface capability which are programmable through an APB interface. The interface to system memory is a 32-bit AHB-Lite master. AHB-Lite is an AMBA bus protocol specification used to connect an AHB master to multiple AHB slaves, typically connecting to ARM or AHB-Lite compatible processor systems such as the SPARC, MicroBlaze and Zynq processors (using Xilinx AXI to AHB-Lite/APB conversion interface).

SpaceWire AHB-Lite DMA IP

Functions

The IP core is comprised of an AHB-Lite master interface, an APB slave interface, up to 2 bi-directional programmable DMA channels, a set of control and status registers, and an Interrupt controller and vector for system interrupts.

An overview of the IP functional blocks is shown below.



AHB-Lite DMA IP Core function overview

Each DMA channel has a transmit and receive data path.

The data paths are described in the transmit and receive sections below.

DMA Transmit

The DMA transmit data path can be programmed to send one or more SpaceWire packets using descriptor lists.

The transmitter is comprised of a FIFO which supports AHB-Lite burst transfers, a set of user accessible registers, a controller and a CRC generator.

The transmit controller can build a SpaceWire packet from one or more data buffers stored in system memory. Each data buffer has an associated descriptor which is stored in system memory. Descriptor lists are used by software to set the location and properties of the transmission of data buffers as SpaceWire packets. Each descriptor includes a pointer to the buffer and a set of flags which determine the length and the type of the SpaceWire packet data generated.

Transmission of SpaceWire RMAP, CCSDS PUS or other protocol packets is supported by providing the hardware computation of CRC-8 or CRC-16 fields. Header and data CRC calculation is supported using multiple data chunks.

The controller can support single-shot or continuous transmission of packets.

In single-shot mode the transmitter sends a list of packet chunks followed by a completion interrupt.

Continuous transmission is an extension of the single-shot mode where the interrupt is generated when part of the list of packet chunks have been sent, therefore freeing up resources to send new packets. The transmitter can interrupt without halting the actual operation. This makes it possible to achieve the maximum SpaceWire data rate with minimum CPU utilisation.

DMA Receive

The DMA receive data path can be programmed to receive one or more SpaceWire packets to a user defined area of system memory. The receiver uses a descriptor table and data buffer in system memory to store new packet data and to describe the stored data in an efficient list for software interaction. Each descriptor indicates the address of new packet data, the length set of descriptors stored in system memory to indicate when new packet data is received, the length and the type of packet.

Packets which are received on the same DMA channel are stored contiguously in memory and their packet length is stored in packet descriptors.

Reception of RMAP packets is supported by providing the hardware computation of its CRC-8. Similarly, CCSDS PUS packets are supported by providing the hardware computation of CRC-16.

Single-shot reception of packets is provided using a number of descriptors before interrupt count which can be set by software for the expected data size and number of descriptors.

Continuous reception of packets is provided using a circular buffer architecture with data and packet descriptor pointers. Interrupts can be set to monitor the progress of packets received without halting the actual operation. The user application or the software driver should free the space used by packets already processed. This procedure allows data to be received at the maximum SpaceWire data rate with minimum CPU utilisation.

Each receiver DMA channel has an associated interrupt bit which can be set to indicate the progress of packets received. The interrupt can indicate when receive errors or events occur including CRC error, EEP received, descriptor space full and data space full.

When an error occurs, the reception is halted and a system interrupt can be raised if enabled.

SpaceWire Port

The SpaceWire port is a STAR-Dundee SpaceWire IP core which implements the SpaceWire serial protocol. The SpaceWire port is

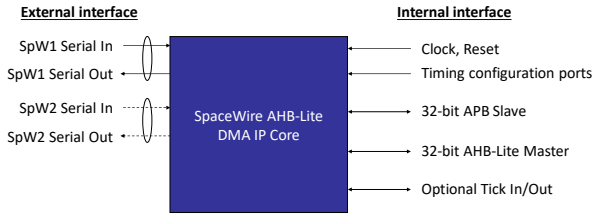
accessed through the register interface, including the link control and the link status interface.

A Time-code transmit and receive interface is provided in the register set or through the IP interface.

An interrupt can be generated on user selected status events such as link errors, link initialisation or Time-code received.

Interfaces

The IP core interfaces are shown below.



AHB-Lite DMA Core interfaces

The internal interface to the application is comprised of:

- SpaceWire interface timing configuration for state machine timeouts and disconnect timeouts. Static values are typically set before netlist generation.
- Register access 32-bit APB slave interface which implements the APB 3.0 interface.
- DMA Data transfer 32-bit AHB-Lite master interface.
- Optional Tick In/Out interface for applications where a Time-code function is required. Internal register interface is also supported.

The external interface is comprised of:

- SpaceWire serial interface for SpaceWire port 1 and the optional SpaceWire port 2. SpaceWire port 2 can be used as a second DMA channel or as a redundant SpaceWire interface port.

Features

The IP provides a highly flexible interface between an AHB-Lite/APB compatible system and a SpaceWire network. The IP has the following features:

- SpaceWire port with 32-bit AHB-Lite master interface and APB slave register interface.
- Powerful DMA controller which simplifies data transfer between buffers in system memory and SpaceWire packets sent/received on the SpaceWire link.
- Hardware CRC generation and checking for RMAP, PUS or user protocol support.
- Maskable interrupt which provides DMA channel status and SpaceWire interface status, including link initialisation and Time-code reception.
- Configurable clocking and Encoder Double Data Rate (DDR) option compatible with technology specific FPGA buffers.
- Compliant with the SpaceWire standard, ECSS-E-ST-50-12C including link-level error recovery scheme from clause 11.
- Internal FIFO storage instantiation in Fabric TMR protected flip-flops, HDL inferred RAM blocks, EDAC protected RTG4 uSRAM using RTG4 RAM64x18 primitives with ECC enabled or EDAC protected ProASIC3 SRAM using a Microchip CoreEDAC core.
- Configurable transmitter and receiver FIFO size. Up to 64 bytes when using the RTG4 uSRAM 64x18 SRAM blocks. Up to 512 bytes when using the ProASIC3 512x18 SRAM blocks and dedicated Microchip CoreEDAC core. Unlimited size when inferred memory instances are used.

Performance and Statistics

The approximate utilisation figures using the reference design implementation is given in the table below. Xilinx FPGA results are obtained using XST or Vivado Synthesis. Microchip results are obtained using Synplify synthesis. Contact enquiries@star-dundee.com for further information on devices which are not listed.

Technology	Comb	FF	RAM
Xilinx Zynq, 7-Series, UltraScale, UltraScale+	Contact STAR-Dundee		
Microchip ProASIC3 (E/L) – pre TMR	Contact STAR-Dundee		
Microchip RTG4/SmartFusion2/Igloo2	1970	943	4
NanoXplore NG-Medium	Contact STAR-Dundee		

Licensing

STAR-Dundee IP cores are available under license, provided as complete VHDL source code.

STAR-Dundee offers essential SpaceWire interface and network components as VHDL IP blocks for use in FPGAs and ASICs. Our IP has proven to be robust and is widely used across the space industry, having been integrated into a number of flight FPGAs and flight ASICs.

Each of our SpaceWire IP cores has the following features:

- Delivered as synthesisable VHDL source code in obfuscated or clear code format.
- Configurable, giving flexibility through generics in the VHDL source.
- Easily targeted for major FPGAs including Microchip, Xilinx, Altera and NanoXplore. Support for radiation tolerant device features included in the Microchip RTAX, ProASIC3L and RTG4.

Reference designs are available for Microchip RTG4 and Xilinx UltraScale development kits. Please contact STAR-Dundee for other devices.

For more information on the IP cores, licenses, or if you have specific or custom requirements, please contact us.

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