SpaceFibre IP Core

SpaceFibre (SpFi) is a very **high-speed serial link** designed specifically for use onboard spacecraft. The aim of SpaceFibre is to provide **point-to-point and networked interconnections** for **Gigabit rate** instruments, mass-memory units, processors and other equipment, on board a spacecraft. SpaceFibre carries **SpaceWire packets** over virtual channels and provides a **broadcast** feature similar to SpaceWire time-codes but offering much more capability. SpaceFibre operates at more than 10 times the data-rate of SpaceWire and can run over fibre optic (long distances) or copper media (less than 10 m).

SpaceFibre is compatible with the packet level of the SpaceWire standard (ECSS-E-ST-50-12C). This means that applications developed for SpaceWire can be readily transferred to SpaceFibre. SpaceFibre is in the final stage of becoming an ECSS standard.

Quality of Service Control and Error Recovery

The SpaceFibre standard defines a medium access controller (MAC) that determines which channels can send data and in which order. The Quality of Service (QoS) is independently configurable for each Virtual Channel. The following mechanisms can be configured and combined:

- Scheduling
- Priority
- Bandwidth Reservation

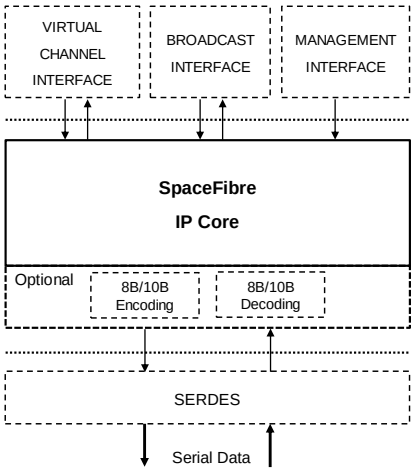
SpaceFibre has an **error recovery mechanism** that automatically recovers from transient and persistent errors on the SpaceFibre link.

IP Core Features

The STAR-Dundee SpaceFibre IP core has the following general features:

- Compliant with the SpaceFibre standard. Supports all the standard functionality including **multi-laning** (which is available in a separate IP Core).
- Dedicated TLK2711 (**Wizardlink**) interface, plus regular standard SerDes interfaces (with or without 8B/10B capabilities).
- Designed by the same team who created the standard.
- Optimised for low latency operation.
- Highly configurable, giving flexibility through generics in the VHDL source. The following characteristics can be configured:
  - Addition of embedded 8B/10B codec
  - Loopback mode
  - Number of **Virtual Channels**
  - Size of the Virtual Channel buffers
  - Lane rate (e.g. 2.5 / 3.125 / 6.25 Gbps, etc.)
- The Quality of Service parameters can be configured in real time during operation.
- Simple data and broadcast interfaces based on standard input and output FIFO interfaces (**AXI4-Stream**).
- Independent data read and write clocks. The user can use arbitrary speeds to write and read from data interfaces.
- Automatically recovers from transient errors in less than 4µs, without affecting the user data rate. Includes BER monitoring.
- Possibility to start one end of the link in a low-power mode waiting for the other end to become active.
- Status and error reporting.
- Data and broadcast babbling idiot protection.
- Validated in major FPGA families including radiation hard devices such as the Microsemi RTG4 and RTAX family.

The I/O of the SpaceFibre IP Core can natively interface with a TLK2711 space qualified SerDes, and can interface to a SerDes with or without 8B/10B capability (see Figure). Furthermore, STAR-Dundee also provides stand-alone IP Cores for specifically interfacing to several FPGA families such as the **RTG4, RTAX, Virtex**, **Kintex**, **Zynq**, etc. A block diagram of the interconnection of the IP Core is shown below.



Resources Required

The resources required by a SpaceFibre design in the RTG4 with transmit and receive FIFOs are detailed below for versions with 1, 2 and 4 Virtual Channels.

	RTG4 *		
	LUT	**DFF**	**RAM Block**
SpFi 1 VC	3700 (2.4%)	2585 (1.7%)	4 (2%)
SpFi 2 VC	3970 (2.6%)	3100 (2.0%)	6 (3%)
SpFi 4 VC	6950 (4.5%)	3760 (2.5%)	10 (5%)

* 8B/10B encoding performed inside the IP Core

Licensing

STAR-Dundee SpaceFibre IP is available under license.

For more information on the IP cores, license, or if you have specific or custom requirements, please contact us.

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