STAR-Dundee

SpaceWire and SpaceFibre Expertise

RMAP IP Cores

RMAP (Remote Memory Access Protocol) provides a standard mechanism for reading from and writing to memory or registers in a remote SpaceWire or SpaceFibre node. This simple but powerful capability is already designed into many components, like the SpW-10X router and missions like BepiColombo. RMAP is an ECSS standard (ECSS-E-ST-50-52C).

SpaceWire (ECSS-E-ST-50-12C Rev.1) is a data-handling network for use on-board spacecraft, which connects instruments, mass memory, processors, downlink telemetry, and other on-board subsystems. SpaceWire has some specific characteristics that help it support data-handling applications in space.

SpaceFibre (ECSS-E-ST-50-11C) is a very high-speed serial data-link intended for use in data-handling networks. It can operate over fibreoptic and electrical cables and can support data rates greater than 6.25 Gbit/s. It aims to complement the capabilities of the widely used SpaceWire standard: improving the data rate by a factor of 15, reducing the cable mass and providing galvanic isolation. The use of SpaceFibre's multi-lane capabilities provides data rates of over 50 Gbit/s for high data-rate payloads.

STAR-Dundee offers essential SpaceWire and SpaceFibre interface and network components such as VHDL IP blocks for FPGAs and ASICs. Our IP cores have been demonstrated to be robust and are widely used across the space industry, having been integrated into flight designs for FPGAs and ASICs.

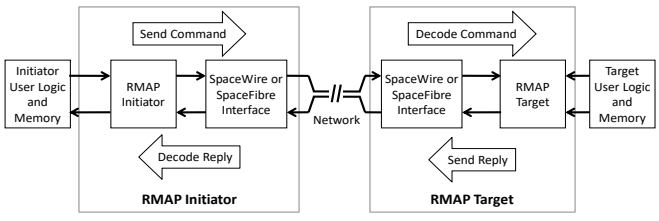
RMAP IP Cores

STAR-Dundee provides two IP cores that together implement the RMAP standard. The cores are listed below:

- RMAP Initiator IP core
- RMAP Target IP core

Both RMAP IP cores are compatible with the STAR-Dundee SpaceWire and SpaceFibre Interface IP cores.

The separation of the functionality of the Initiator IP core and the Target IP core is illustrated below. Combined, they provide a full RMAP link.



RMAP Initiator IP Core

The RMAP transaction encoding and decoding function is provided by the RMAP Initiator IP core. The initiator user logic sets up a transaction table, a set of RMAP transaction parameters, the data buffers for the transactions and the notification buffers in system memory. It instructs the RMAP Initiator IP core to start one or more RMAP transactions from a command list. The transactions are executed by the IP core and encoded as RMAP command packets to be transmitted over the SpaceWire or SpaceFibre Interface.

The Initiator IP supports posted commands using a transaction table. It keeps a record of the outstanding write transactions which are acknowledged and read or read-modify-write commands which return data. An optional timeout can check if a transaction has not been completed within a user-specified period.

On reception of a packet, the RMAP Initiator decodes the reply packet and then searches for the transaction in the outstanding transactions table. If the transaction is valid and its fields are matched, any read or read-modify-write data is written to system memory. The notification buffer is updated with the transaction status and the transaction is removed from the outstanding transactions table.

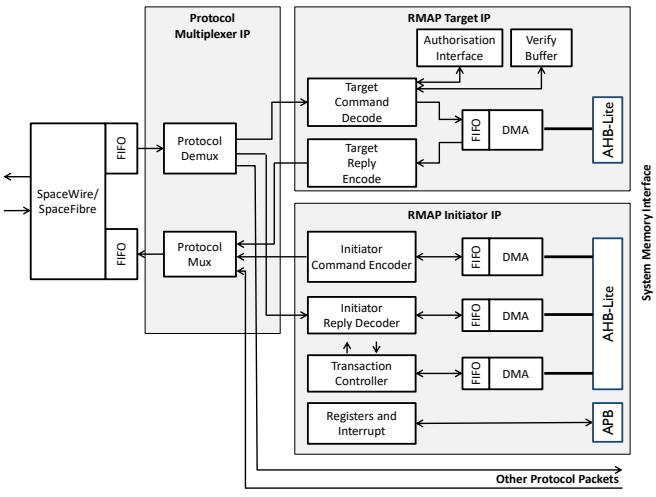
RMAP Target IP Core

The command decoding and remote memory access function is provided by the RMAP Target IP core. RMAP packets are received and decoded by the Target IP. If the RMAP command is a valid command packet, the parameters of the command are passed to the authorisation interface. If the command is authorised, the Target IP core will write the command data to the user system memory or read data from the user system memory to be sent back to the initiator. Read-modify-write operation is supported where data is read from memory, modified by a user defined function, then written back to memory.

The Target IP core formats an RMAP reply packet for write commands which require acknowledgement or for read and read-modify-write commands with returned data.

Architecture

A summary of the RMAP IP core architecture, including both Initiator and Target IP cores, is shown in the following figure.



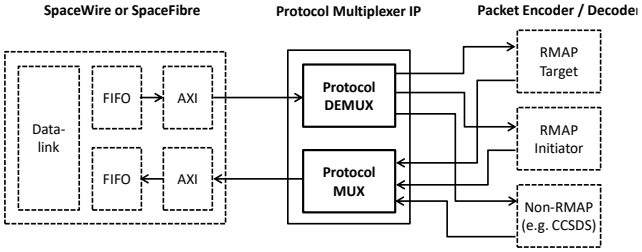
A description of the architecture blocks is provided in the following list.

- The SpaceWire or SpaceFibre interface core implements the ECSS data transfer protocol.
- A protocol decoder and multiplexer module checks the packet header for RMAP compliant packets to determine the packet destination. The module can be disabled when the serial interface only handles RMAP packets.
- The RMAP Target units decode RMAP command packets, check for command authorisation, read or write data from or to system memory, and encode RMAP reply packets.

- The RMAP Initiator units accept commands into the transaction table, encode RMAP command packets, decode reply RMAP packets, access data buffers in system memory, and output status information. The initiator is programmed via an APB register programming interface.
- The protocol decoder and multiplexer module has a non-RMAP packet interface which allows user logic to receive or transmit other telecommand or telemetry packets if required.

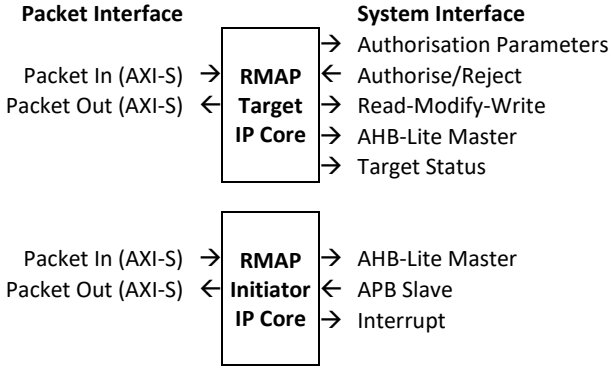
Protocol Multiplexer

A protocol multiplexer IP core is provided with the RMAP IP cores. It is a standalone IP core which can be instantiated between a SpaceWire interface or SpaceFibre virtual channel and the RMAP IP. It has a basic function to act as an RMAP packet aware multiplexer to support both RMAP command and reply packet formats, and to pass all other traffic through a non-RMAP interface. It can be used to combine RMAP traffic and other data packet formats. A summary of the functions provided by the protocol multiplexer is shown in the following figure.



Interfaces

The RMAP IP core interfaces are shown in the following figures. The SpaceWire, SpaceFibre and RMAP IP cores use AXI-Stream encoding interfaces to move packet data. The RMAP IP cores use the AHB-Lite protocol to access system memory.



IP Core Features

The RMAP IP cores have the following features:

- Compliant with the SpaceWire RMAP ECSS-E-ST-50-52C standard.
- Delivered as synthesisable VHDL source code in obfuscated or clear code format.
- Configurable, supporting target device capabilities and application requirements.
- Supported on Microchip, Xilinx, Intel, Lattice, and NanoXplore FPGAs.
- Support for radiation-tolerant device features included in Microchip RTAX, ProASIC3E/L, RTG4 and RT-PolarFire, and Xilinx Kintex UltraScale and Versal FPGAs.
- Documented example designs are available for Xilinx, Microchip, Lattice and NanoXplore devices. Please contact us for other target devices.

Testing

The RMAP Target and RMAP Initiator IP cores have been extensively tested using a VHDL testbench and hardware tests, covering many possible configurations and error conditions.

Both IP cores are provided with a VHDL testbench which performs common interface operations including initialisation and reset, non-RMAP packet transfer, and RMAP command and response transfers.

Device Utilisation

The utilisation figures for a typical RMAP IP implementation with a 32-bit AHB-Lite bus interface and 8-beat burst FIFOs is given in the tables below. The protocol multiplexer is enabled.

The Xilinx FPGA results were obtained using Vivado Synthesis.

The Microchip results were obtained using Synplify Synthesis. In addition to the Microchip FPGAs listed below, ProASIC3 and RTAX devices are also supported. Please contact us for further details on these or other FPGAs (NanoXplore, Lattice, Intel, etc.)

RMAP Target IP core utilisation

Technology	LUT	FF	RAM
Xilinx 7-Series, Zynq, UltraScale, UltraScale+, Versal	1401	1108	2
Microchip RTAX	2769	1273	2
Microchip ProASIC3 (Core cells, TMR Enabled)	15165		8
Microchip RTG4, IGLOO2, SmartFUSION2	2081	1119	2
Microchip PolarFire (TMR enabled)	4119	3546	2

RMAP Initiator IP core utilisation

Technology	LUT	FF	RAM
Xilinx 7-Series, Zynq, UltraScale, UltraScale+, Versal	2897	1698	5
Microchip RTAX	5569	2458	5
Microchip ProASIC3 (Core cells, TMR Enabled)	27240		17
Microchip RTG4, IGLOO2, SmartFUSION2	4567	5301	5
Microchip PolarFire (TMR enabled)	8228	6864	5

Licensing

STAR-Dundee RMAP IP cores are available under license, provided as synthesisable VHDL source code.

For more information on the IP cores, licensing, or if you have specific or custom requirements, please contact us.

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