STAR-Dundee

SpaceWire Engineering Excellence

SpaceFibre IP Cores

SpaceFibre (SpFi) is a very **high-speed serial link** designed specifically for use onboard spacecraft. The aim of SpaceFibre is to provide **point-to-point and networked interconnections** for **Gigabit rate** instruments, mass-memory units, processors and other equipment, on board a spacecraft. SpaceFibre carries **SpaceWire packets** over virtual channels and provides a **broadcast** feature similar to SpaceWire time-codes but offering much more capability. SpaceFibre operates at more than 15 times the data-rate of SpaceWire and can run over fibre optic (long distances) or copper media (less than 10 m).

SpaceFibre is compatible with the packet level of the SpaceWire standard (ECSS-E-ST-50-12C). This means that applications developed for SpaceWire can be readily transferred to SpaceFibre. SpaceFibre is in the final stage of becoming an ECSS standard.

SpaceFibre Single-Lane IP Core

This IP is fully compliant with the SpaceFibre standard except for the Multi-Lane layer which is available as a separate IP (see next page).

Quality of Service Control and Error Recovery

The SpaceFibre standard defines a medium access controller (MAC) that determines which Virtual Channels can send data and in which order. The Quality of Service (QoS) is independently configurable for each Virtual Channel. The following mechanisms can be configured and combined:

- Scheduling
- Priority
- Bandwidth Reservation

SpaceFibre has an **error recovery mechanism** that automatically recovers from transient (recovery in less than 2 µsec) and persistent errors on the SpaceFibre link.

Single-Lane IP Core Features

The STAR-Dundee SpaceFibre Single-Lane IP core has the following features:

- Compliant with the SpaceFibre standard. Supports all the standard functionality except Multi-Lane (separate IP Core).
- Designed by the same team who created the standard.
- **Easy to use** with a protocol agnostic interface. No prior knowledge of SpaceFibre standard is required. The SpaceWire packet size, format and content is arbitrary.
- Dedicated TLK-2711 (**Wizardlink**) interface, plus regular standard SerDes interfaces (with or without 8B/10B capabilities).
- Optimised for low latency operation.
- 80-bit broadcast interface for **ultra-low latency short messages** (< 400 ns).
- Highly configurable, giving flexibility through generics in the VHDL source. The following characteristics can be configured:
  - Addition of inbuilt 8B/10B codec
  - Number of **Virtual Channels**
  - Size of the Virtual Channel buffers
- Support lane rates up to **3.125 Gbit/s in RTG4 or Virtex-5QV**.
- Guaranteed timing closure in RTG4 or Virtex-5QV with EDAC and SET filter enabled and worst-case conditions.
- The Quality of Service parameters can be configured in real time during operation.
- Simple data interfaces based on standard input and output FIFO interfaces (32-bit **AXI4-Stream**).
- Independent user-defined data read and write AXI clocks.
- Automatically recovers from transient errors in less than 2 µs, without affecting the user data rate.
- Possibility to start one end of the link in a low-power mode waiting for the other end to become active.
- Data and broadcast babbling idiot protection.
- Data integrity and reliable data delivery for BER better than 10^{-5} and automatic lane disconnection when BER is worse than 10^{-5}.
- Very simple management interface, with optional statistics and debug signals.
- Validated in major FPGA families including radiation hard devices, e.g. Microsemi RTG4 and RTAX, and Xilinx Virtex-5QV.

The IP is natively compatible with RTG4 and Xilinx (e.g. Virtex-5QV) using their inbuilt high-speed SerDes blocks. SpFi can interface to a SerDes with or without 8B/10B capability. Only four FPGA pins (two differential pairs) are required per SpFi lane. The configuration of the SerDes interface depends on the FPGA:

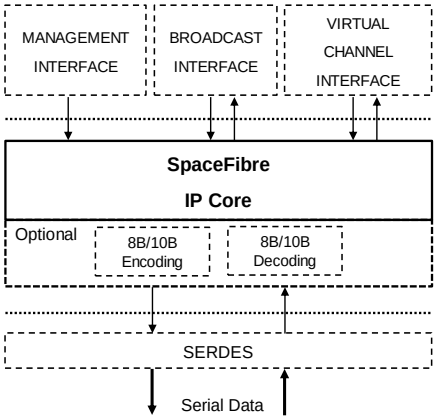
RTG4 interface:

- 8B10B encoding (20-bit interface), clock correction and symbol alignment done inside the IP Core.
- Three clocks required, lane rate/20 and lane rate/40 for TX and the recovered clock lane rate/20 for RX.

Xilinx interface:

- 8B10B encoding (32-bit interface), clock correction and symbol alignment done in the Xilinx transceiver.
- One clock required, lane rate/40 for TX.

An external SerDes is required for older FPGA technologies. The SpaceFibre IP Core can be configured to directly interface with a TLK-2711 space qualified SerDes. Furthermore, STAR-Dundee also provides stand-alone IP Cores for specifically interfacing to several FPGA families such as the **RTG4, RTAX, Virtex**, **Kintex**, **Zynq**, etc. A block diagram of the interconnection of the IP Core is shown below.



Resources Required

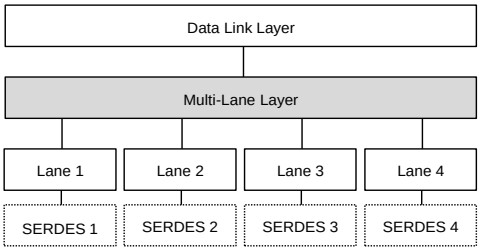
The RTG4/Virtex-5QV resources required by the SpaceFibre module including transmit and receive FIFOs are detailed below for different Virtual Channels.

	RTG4 [1]			Virtex-5QV		
	LUT	DFF	RAM Block [2]	LUT	DFF	RAM Block
1 VC	3944 2.6%	2818 1.9%	4 1.9%	2750 3.4%	2365 2.9%	4 1.3%
2 VC	4454 2.9%	3197 2.1%	6 2.9%	3138 3.8%	2596 3.2%	6 2.0%

[1] 8B/10B encoding performed inside the IP Core
[2] Only RAM1K18 blocks are used. No RAM64x18 blocks are required

SpaceFibre Multi-Lane IP

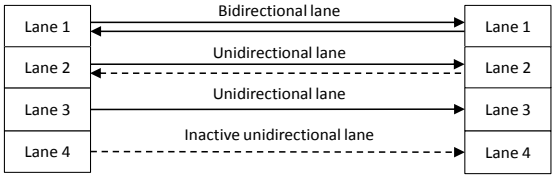
Multi-Lane is an optional capability of the SpaceFibre link defined in the SpaceFibre protocol stack. The Multi-Lane layer is defined between the Data Link layer and the Lane layer implemented for each available lane.



The Multi-lane layer coordinates the operation of multiple lanes as a single SpaceFibre link, providing higher data throughput and redundancy. Because the logic to initialise a lane and monitor its status is located below the multilane layer, each lane can be initialised and operated independently of each other.

This architecture supports automatic graceful degradation, spreading traffic over the remaining working lanes automatically in the event of a lane failure and, thanks to the QoS, with higher priority VCs being less affected. Bandwidth overprovision and dynamic power management is also possible. These capabilities are very useful for space applications.

Single-Lane SpaceFibre implementations must be bidirectional even if the end-user data flow is unidirectional, because of the feedback required by the protocol. However in a Multi-Lane implementation only one bidirectional lane is enough for protocol related information. Therefore, other lanes can be unidirectional, saving power and mass.



In this 4-lane configuration example, bidirectional lane 2 can be set to a unidirectional lane for power saving reasons. Unidirectional Lane 4 can be enabled when one lane fails or a higher data rate is required. It is also possible to send data using all four lanes and add an additional one configured as a hot redundant lane, which only sends data when another lane fails.

Multi-Lane IP Core Features

The STAR-Dundee SpaceFibre Multi-Lane IP core has been designed to be easy to use, with minimum configuration signals. On top of the features of the Single-Lane IP Core, the Multi-Lane IP also features:

- Configurable number of independent lanes with cold and hot redundancy. Any number of lanes supported (up to 16).
- Automatic graceful degradation when link BW is reduced, with higher priority Virtual Channels being less affected.
- Hot redundant lanes recover from lane failures in less than 2 µs without user intervention.
- Lanes can be configured as unidirectional to save power and mass in asymmetric data flows.
- Wide AXI4-Stream interface to support slow user clock.
- Support lane rates up to **3.125 Gbit/s in RTG4 or Virtex-5QV** (e.g. aggregate rates of up to 6.25 Gbit/s using 2 lanes or up to 12.5 Gbit/s using 4 lanes).
- Guaranteed timing closure with EDAC and SET filter enabled and worst-case conditions.

Resources Required

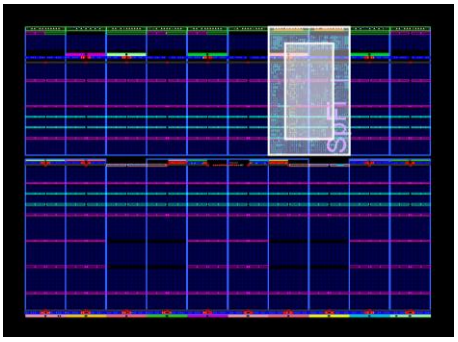
The resources required by a SpaceFibre design in RTG4/Virtex-5QV including transmit and receive FIFOs are detailed below for different number of lanes and Virtual Channels.

	RTG4 [1]			Virtex-5QV		
	LUT	DFF	RAM Block [2]	LUT	DFF	RAM Block
2 Lanes 1 VC	6494 4.3%	5351 3.5%	8 3.8%	3858 4.7%	3938 4.8%	8 2.7%
2 Lanes 2 VC	7314 4.8%	6088 4.0%	12 5.7%	4503 5.5%	4382 5.3%	12 4.0%
3 Lanes 2 VC	8997 5.9%	7413 4.8%	12 5.7%	5416 6.6%	5226 6.4%	12 4.0%

[1] 8B/10B encoding performed inside the IP Core
[2] Only RAM1K18 blocks are used. No RAM64x18 blocks are required

IP Core Delivery Files

The STAR-Dundee SpaceFibre IP Cores come with a reference design for RTG4 (Libero) and Virtex-5QV (ISE) that can directly be implemented in the FPGA for easy adoption. There is also an comprehensive end-user test bench for Modelsim/Questa simulators.



Licensing

STAR-Dundee SpaceFibre Single-Lane and Multi-Lane IP Cores are available under license. For more information on the IP cores, license, or if you have specific or custom requirements, please contact us.

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