STAR-Dundee

SpaceWire and SpaceFibre Expertise

SpaceFibre Interface IP Core

SpaceFibre (SpFi) is a very **high-speed serial link** designed specifically for use onboard spacecraft (ECSS-E-ST-50-11C). SpaceFibre provides **point-to-point and networked interconnections** for **Gigabit rate** instruments, mass-memory units, processors and other equipment, onboard a spacecraft. SpaceFibre encapsulates information in packets which have the same format and addressing scheme as **SpaceWire.** Packets flow over virtual channels which support Quality of Service. SpaceFibre also has a low latency **broadcast message** capability which can broadcast short messages to all nodes on a network. SpaceFibre operates at more than 15 times the data rate of SpaceWire and can run over fibre optic (long distances) or copper media (several metres).

SpaceFibre is compatible with the packet level of the SpaceWire standard (ECSS-E-ST-50-12C). This means that applications developed for SpaceWire can be readily transferred to SpaceFibre.

SpaceFibre is a data and control plane technology in the latest **SpaceVPX standard** (ANSI/VITA 78.0 2022) and the high-speed interconnect in the emerging ESA **ADHA standard**.

The STAR-Dundee SpaceFibre Interface IP Core has been successfully **tested under radiation** in collaboration with Microchip. The IP Core can be implemented in radiation-tolerant **ASIC** technologies and has **flight heritage**, as it has been deployed in several operational space missions (**TRL-9**).

SpaceFibre Single-Lane Interface IP Core

The SpaceFibre Interface IP Cores are fully compliant with the SpaceFibre standard. The Multi-Lane layer is available as a separate IP core (see next page).

Quality of Service Control and Error Recovery

The SpaceFibre standard defines a medium access controller (MAC) that determines which virtual channels can send data and in which order. The Quality of Service is independently configurable for each virtual channel. The following Quality of Service mechanisms, which can be configured and combined, are included:

- Scheduling
- Priority
- Bandwidth Reservation

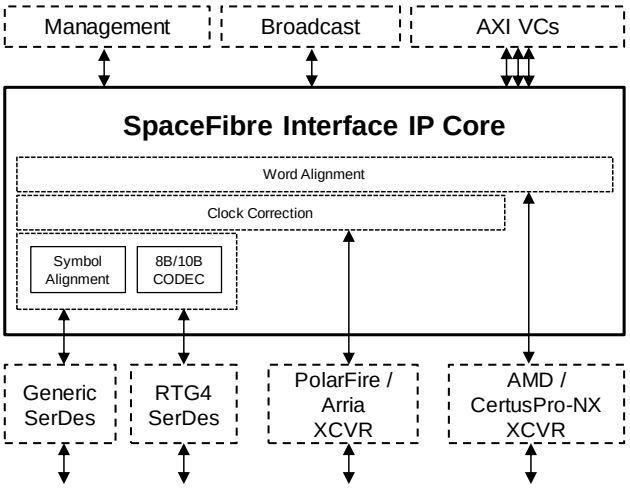
SpaceFibre has an **error recovery mechanism** that automatically recovers from transient and persistent errors on the SpaceFibre link, with recovery from transient errors in less than 3 microseconds.

Single-Lane Interface IP Core Features

The STAR-Dundee SpaceFibre Single-Lane Interface IP core has the following features:

- Compliant with the SpaceFibre standard (**ECSS-E-ST-50-11C**).
- Technology independent (FPGA or ASIC) and optimised for radiation-hardened FPGAs.
- Designed by the same team who created SpaceFibre.
- **Easy to use**, providing a protocol agnostic interface. No prior knowledge of the SpaceFibre standard is required. The packet size, format and content is arbitrary.
- Configurable target technology (RTG4, PolarFire, UltraScale, Versal, Arria, Certus, generic options) for memory blocks and SerDes interface.
- Optimised for low latency operation.
- 80-bit broadcast interface for **ultra-low latency short messages** (< 400 ns).
- Highly configurable, giving flexibility through generics in the VHDL source, e.g. number of virtual channels and size of internal buffers.
- Support for lane rates of up to **3.125 Gbit/s in RTG4** and **more than 6.25 Gbit/s in PolarFire, Kintex UltraScale or Versal**.
- Timing closure in RTG4 with EDAC and SET filter enabled and worst-case conditions.
- The quality of service parameters can be configured in real time during operation.
- Simple data interfaces based on standard input and output FIFO interfaces (32-bit **AXI4-Stream**).
- Independent user-defined data read and write AXI clocks.
- Automatically recovers from transient errors in less than 3 microseconds, without any significant reduction in user data rate.
- Able to start one end of the link in a low-power mode waiting for the other end to become active.
- Data and broadcast babbling node protection.
- Data integrity and reliable data delivery for Bit Error Rate (BER) better than 10^{-5} and automatic lane disconnection when BER is worse than 10^{-5}.
- Very simple management interface, with optional statistics and debug signals.

The IP is natively compatible with Microchip devices (e.g. RTG4, PolarFire), AMD devices (e.g. Kintex UltraScale, Versal), and Intel Arria and Lattice CertusPro-NX FPGAs using their inbuilt high-speed SerDes blocks. SpaceFibre can interface to a SerDes with or without 8B/10B capability. Only four FPGA pins (two differential pairs) are required per SpaceFibre lane. The configuration of the SerDes interface depends on the FPGA.



RTG4 interface:

- 8B10B encoding (20-bit interface), clock correction and symbol/word alignment performed inside the IP Core.
- Three clocks required, lane rate/20 and lane rate/40 for TX and the recovered clock lane rate/20 for RX.

PolarFire / Arria interface:

- 8B10B encoding (32-bit interface) and symbol alignment performed inside the IP Core.
- Clock correction and word alignment performed inside the IP Core.
- Two clocks required, lane rate/40 for TX and the recovered clock lane rate/40 for RX.

AMD / CertusPro-NX interface:

- 8B10B encoding (32-bit interface), clock correction and symbol/word alignment performed in the AMD transceiver.
- One clock required, lane rate/40.

An external SerDes is required for older FPGA technologies. The SpaceFibre IP Core can be configured to directly interface with a TLK2711 space-qualified SerDes.

Resources Usage

The resources required by a SpaceFibre design depend on the specific FPGA in use and the user configuration. The tables below show the percentage of total resource usage for different numbers of virtual channels (VCs). The values in the tables include the transmit and receive FIFOs.

	RTG4			XQRKU060 [1]		
	LUT	**DFF**	**RAM**	**LUT**	**DFF**	**RAM**
1 VC	2.0%	1.5%	1.9%	0.5%	0.3%	0.4%
2 VC	2.4%	1.8%	2.9%	0.6%	0.4%	0.6%
4 VC	3.2%	2.6%	4.8%	0.9%	0.6%	0.9%

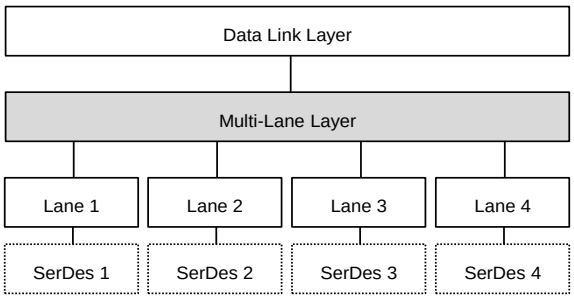
	RTPF500T [1]			XQRVC1902 [1]		
	LUT	**DFF**	**RAM**	**LUT**	**DFF**	**RAM**
1 VC	0.6%	0.4%	0.5%	0.2%	0.1%	0.4%
2 VC	0.7%	0.6%	0.8%	0.2%	0.2%	0.6%
4 VC	0.9%	0.8%	1.3%	0.3%	0.2%	1.0%

[1] TMR not included

For resource usage when using other configurations please contact STAR-Dundee Support (ip.support@star-dundee.com).

SpaceFibre Multi-Lane Interface IP Core

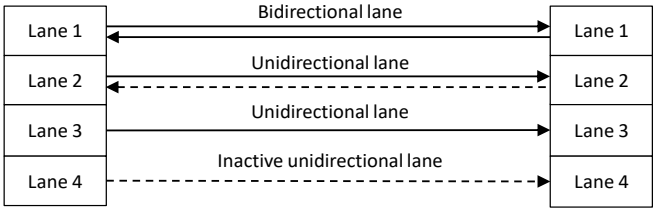
Multi-Lane is an optional capability of the SpaceFibre link, as defined in the SpaceFibre protocol stack. The Multi-Lane layer is defined between the Data Link layer and the Lane layer implemented for each available lane.



The Multi-Lane layer coordinates the operation of multiple lanes as a single SpaceFibre link, providing higher data throughput and redundancy. Because the logic to initialise a lane and monitor its status is located below the Multi-Lane layer, each lane can be initialised and operated independently of each other.

This architecture supports automatic graceful degradation, spreading traffic over the remaining working lanes automatically in the event of a lane failure and, thanks to the Quality of Service mechanisms, with higher priority VCs being less affected. Furthermore, the number of active lanes can be dynamically changed, reducing the power consumption when the full bandwidth is not required. These capabilities are very useful for space applications.

A SpaceFibre link is bidirectional. However, when a multi-lane link is being used and the data flow is mainly in one direction, it is possible to provide more lanes in the direction of the data flow, provided that there is at least one lane in the return direction. This is illustrated in the diagram below where there is one bidirectional lane and some unidirectional lanes. This saves mass and power compared to a link built with only bidirectional lanes.



In this 4-lane example, the bidirectional Lane 2 can be set as a unidirectional lane for power saving reasons. Unidirectional Lane 4 can be enabled when one lane fails or a higher data rate is required. It is also possible to send data using all four lanes and add an additional lane configured as a hot-redundant lane, which only sends data when another lane fails.

Multi-Lane Interface IP Core Features

The STAR-Dundee SpaceFibre Multi-Lane Interface IP core has been designed to be easy to use, with minimum configuration signals. In addition to the features of the Single-Lane IP Core, the Multi-Lane IP also provides:

- Configurable number of independent lanes with warm- and hot-redundancy. Any number of lanes supported (up to 8).
- Automatic graceful degradation when link bandwidth is reduced, with higher priority virtual channels being less affected.
- Hot-redundant lanes recover from lane failures in less than 3 microseconds without user intervention.
- Lanes can be configured as unidirectional to save power and mass in asymmetric data flows.
- Wide AXI4-Stream interface to support slow user clock.
- Support for lane rates of up to **3.125 Gbit/s in RTG4** (e.g. aggregate rates of up to 25 Gbit/s with 8 lanes) or **more than 6.25 Gbit/s in PolarFire, Kintex UltraScale or Versal** (e.g. aggregate rates of up to 50 Gbit/s with 8 lanes).

Resources Usage

The resources required by SpaceFibre designs with different numbers of lanes and virtual channels (VCs) are detailed below for different technologies. These values include the transmit and receive FIFOs.

		RTG4			XQRKU060 [1]		
		LUT	DFF	RAM	LUT	DFF	RAM
2 Lanes	1 VC	4.5%	3.6%	3.8%	0.9%	0.7%	0.7%
	2 VC	5.0%	4.1%	5.7%	1.1%	0.8%	1.1%
	4 VC	6.0%	5.1%	9.6%	1.3%	1.0%	1.9%
4 Lanes	1 VC	8.6%	6.4%	7.7%	1.7%	1.2%	1.1%
	2 VC	9.2%	7.1%	11.5%	1.9%	1.3%	1.7%
	4 VC	10.3%	8.5%	19.1%	2.1%	1.6%	2.8%
8 Lanes	1 VC	18.8%	11.9%	15.3%	3.5%	2.1%	1.9%
	2 VC	19.5%	13.0%	23.0%	3.7%	2.3%	2.8%
	4 VC	21.1%	15.1%	38.3%	4.2%	2.8%	4.6%

		RTPF500T [1]			XQRVC1902 [1]		
		LUT	DFF	RAM	LUT	DFF	RAM
2 Lanes	1 VC	1.1%	0.9%	0.8%	0.3%	0.3%	0.8%
	2 VC	1.3%	1.0%	1.2%	0.4%	0.3%	1.2%
	4 VC	1.6%	1.4%	2.0%	0.5%	0.4%	2.1%
4 Lanes	1 VC	2.1%	1.5%	1.3%	0.6%	0.4%	1.2%
	2 VC	2.3%	1.7%	2.0%	0.6%	0.5%	1.9%
	4 VC	2.6%	2.1%	3.3%	0.7%	0.6%	3.1%
8 Lanes	1 VC	4.7%	2.7%	2.4%	1.2%	0.8%	2.1%
	2 VC	5.0%	3.1%	3.6%	1.3%	0.9%	3.1%
	4 VC	5.4%	3.7%	5.9%	1.4%	1.0%	5.2%

[1] TMR not included

For resource usage when using other configurations please contact STAR-Dundee Support (support@star-dundee.com).

IP Core Delivery Files

The STAR-Dundee SpaceFibre Interface IP Cores come with a reference design for RTG4 and PolarFire (Libero), Kintex UltraScale and Versal (Vivado) that can be directly implemented in the FPGA for easy adoption. Other technologies can be supplied upon request. A comprehensive end user test bench for ModelSim/Questa simulators is also provided.

Licensing

STAR-Dundee SpaceFibre Single-Lane and Multi-Lane Interface IP Cores are available under license. For more information on IP cores, licensing, or for any specific or custom requirements, please contact us at enquiries@star-dundee.com.

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