VHiSSI: Experimental SpaceFibre ASIC

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ABSTRACT

SpaceFibre is the next generation data link and network technology being developed by University of Dundee for the European Space Agency. This high-speed technology runs over both copper and fibre optic cables and is backwards compatible with the ubiquitous SpaceWire technology. SpaceFibre provides 12 times the throughput of a SpW link (2.5 Gbps) with current flight qualified technology together with inbuilt QoS and FDIR capabilities.

This paper details the first implementation of SpaceFibre in a radiation tolerant device in the frame of the VHiSSI project. The functionality of this ASIC chip is explained and the results of the functional and Total Ionising Dose and Single Event Effect radiation testing are detailed.

1 INTRODUCTION

SpaceFibre [1] [2] [3] [4] is the next generation data link and network technology being developed by University of Dundee for the European Space Agency. Currently running at 2.5 Gbps, this high-speed technology runs over both copper and fibre optic cables. SpaceFibre (SpFi) is backwards compatible with the ubiquitous SpaceWire (SpW) [5] technology and provides 12 times the throughput of a SpW link with current flight qualified technology. Thanks to its high speed together with inbuilt QoS and FDIR capabilities, SpFi allows the reduction of system complexity, substantially reducing cable harness mass and simplifying redundancy strategies. SpFi is currently a mature draft standard. An ECSS working group will be convened in 2015 to finalise the standard for formal approval.

2 DESCRIPTION OF VHISSI FUNCTIONALITY

An experimental radiation tolerant SpaceFibre interface device has been developed by University of Dundee, STAR-Dundee, Ramon Chips, ACE-IC, IHP, Airbus DS and SCI within the Very High Speed Serial Interface (VHiSSI) European Commission Framework 7 project. The VHiSSI chip integrates a complete SpaceFibre protocol engine, together with the physical layer interfaces, in a radiation tolerant chip manufactured by a European foundry. A block diagram of the VHiSSI device is shown in Figure 1.

There are six main functions within the VHiSSI chip:

- SpaceWire Bridge
- FIFO, DMA, Memory and Transaction (FIFO/DMT) Interface
- SpaceFibre Interface
- SerDes
- IO Switch Matrix
- Mode Switch Matrix

The SpaceWire Bridge provides a bridge between SpaceWire and SpaceFibre with up to 11 SpaceWire interfaces being available. The SpaceWire Bridge includes a seven port SpaceWire router which allows routing between three SpaceWire ports, three Virtual Channel (VC) buffers of the SpaceFibre interface and a device configuration port. Configuration of the VHiSSI chip can be carried out over any SpaceWire interface connected to the embedded SpaceWire router or over VC0, VC1 and VC2 of the SpaceFibre interface. The SpaceWire Bridge is connected to the IO Switch Matrix and to the Mode Switch Matrix.

The FIFO and DMA, Memory and Transaction (DMT) Interface provides various types of parallel interface into the VHiSSI chip for sending and receiving data over the SpaceFibre interface. The various parallel interface functions have been designed with specific application scenarios in mind and between them are able to operate with many types of local host system, including FPGAs and processors such as the RTC [6] and the Leon2 processor [7]. The parallel interface is also designed to use a small number of pins, so that the VHiSSI chip can fit into a small (100 pin) package.

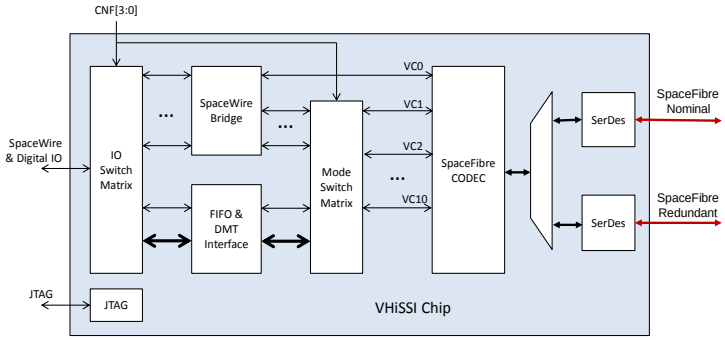

Figure 1 – VHiSSI Chip Block Diagram

The SpaceFibre Interface has 11 virtual channels. VC 0 is intended primarily for VHiSSI device and local system configuration and monitoring and is directly connected to the embedded SpaceWire router. The other SpaceFibre VC buffers are connected to the Mode Switch Matrix which connects them to either the SpaceWire Bridge or the parallel interface depending on the mode of operation. Specifically, VC1 and VC2 are connected to the embedded SpaceWire router or to the parallel interface. The other VCs (VC 3 to VC 10) are connected directly to a SpaceWire interface or to the parallel interface. Each VC supports full SpaceFibre QoS. The QoS can be configured independently for each of the VCs. The SpaceFibre interface is connected via a multiplexer to either the nominal or the redundant SerDes, and then to the CML transceiver.

The SerDes converts parallel data words from the SpaceFibre interface into a serial bit stream and vice versa. On the receive side the bit clock is recovered from the serial bit stream by the SerDes. The SerDes includes integral CML transceivers.

The IO Switch Matrix connects either the SpaceWire LVDS, SpaceWire LVTTL or parallel interface signals from the FIFO and DMT interface to the digital IO pins of the VHiSSI chip. Configuration is static and determined on exit from device reset.

The Mode Switch Matrix connects either the SpaceWire Bridge or FIFO and DMT interface (parallel interface) to the VC buffers of the two SpaceFibre interfaces. Configuration is static and determined on exit from device reset.

The digital logic for VHiSSI was designed by STAR-Dundee Ltd. with system architectural design and project management being carried out by University of Dundee. Airbus DS provided inputs to the VHiSSI requirements. The back end design was carried out by Ramon Chips. ACE-IC designed the SerDes parts of the chip. Test vectors were prepared by STAR-Dundee and SCI with inputs from other partners. The chip was manufactured by IHP. STAR-Dundee was also responsible for the Functional and SEE radiation campaigns while Airbus DS was responsible for the TID radiation campaign. The resulting VHiSSI chip is shown in Figure 2 (layout design) and Figure 3 (final packaged chip).

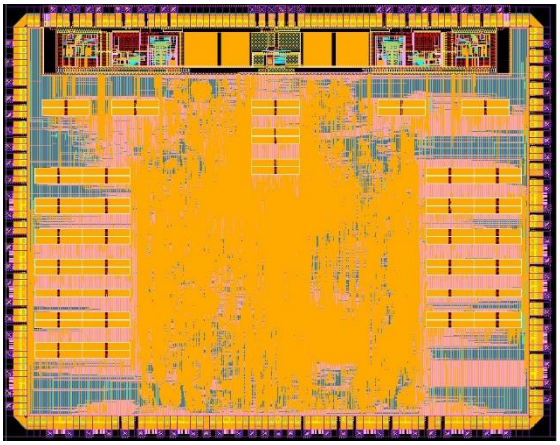

Figure 2 – VHiSSI Chip Layout

Figure 3 – Final VHiSSI Chip

3 FUNCTIONAL TESTING

The three major modes of the VHiSSI have been tested in hardware in the laboratory. The board used for testing the SpaceWire LVTTL bridge mode of operation is shown in Figure 4.

The VHiSSI chip is housed in the centre of the board in a specially designed socket, which has a hole in the top to permit Single Event Effect radiation testing of the VHiSSI device. The 11 SpaceWire links are attached to the front panel of the test board (blue cable) and are concentrated by the VHiSSI chip over the SpaceFibre cable (black cable).

The test set up for this board is illustrated in the Figure 5. Two eight-port SpaceWire routers are used to connect to all the SpaceWire ports of the VHiSSI chip. A STAR Fire unit is connected to the SpaceFibre cable and also to a host computer, via SpaceWire and a SpaceWire-USB Brick. Software on the host computer was written to exercise and test the function of the VHiSSI chip, providing a test report for each device tested.

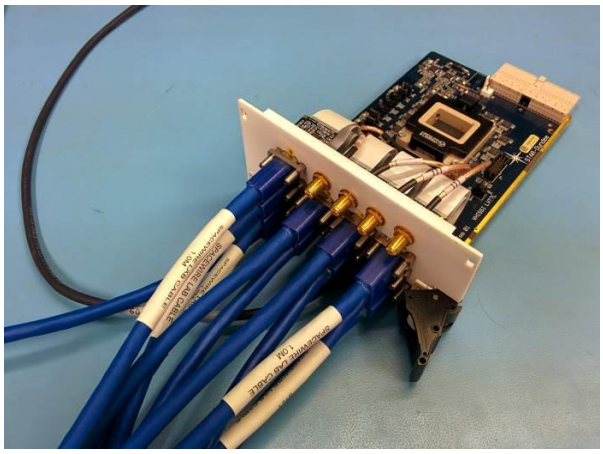

Figure 4 –VHiSSI SpaceFibre to SpaceWire Test Board

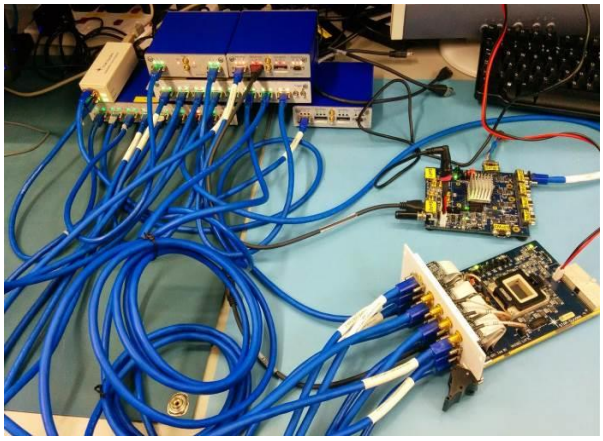

Figure 5 – Test Setup for SpaceWire to SpaceFibre Board

4 TID RADIATION TESTING

VHiSSI implements several mechanisms to minimise the effects of radiation. The chip layout uses a radiation tolerant library developed by Ramon Chips. Moreover, memories feature EDAC allowing to correct single bit-flips and to detect two bit-flips in every memory word.

Figure 6 – VHiSSI TID Testing

The testing of VHiSSI proved the correct operation of the SpFi in an ASIC under representative functional scenarios. Also, the VHiSSI project has provided SpFi with an opportunity to verify its performance under a radiation environment. Total Ionising Dose (TID) and Single Even Effect (SEE) tests have been carried out to assess the behaviour of the chip in realistic space scenarios.

The TID testing has been performed using a 60Co source. In Figure 6 the cylindrical chamber (left) with an example of a test board (right) are shown. Four different chips were tested and no major issues appeared after a dose of 300 kRads. Both analogue and digital parts of the chip were tested. Functional tests showed same behaviour before and after irradiation.

5 SEE RADIATION TESTING

The SEE testing was carried out at the cyclotron of the Université de Louvain La Neuve (CYCLONE) in Belgium. Heavy ions were used in the tests with an energy range between 1 MeV·cm2/mg and 68 MeV·cm2/mg. Figure 7 shows the ion beam entering the radiation chamber. Figure 8 shows the board with VHiSSI in the opened radiation chamber (centre of the picture). In this case, Single Effect Functional Interrupt (SEFI) events were observed above 14 MeV·cm2/mg. Those were non-destructive and power cycling of the board was required to recover functionality. Further testing is required to exactly determine the cause of these events although they are not related to the SpaceFibre operation. Single Event Latch-Ups (SEL) were not observed during the tests.

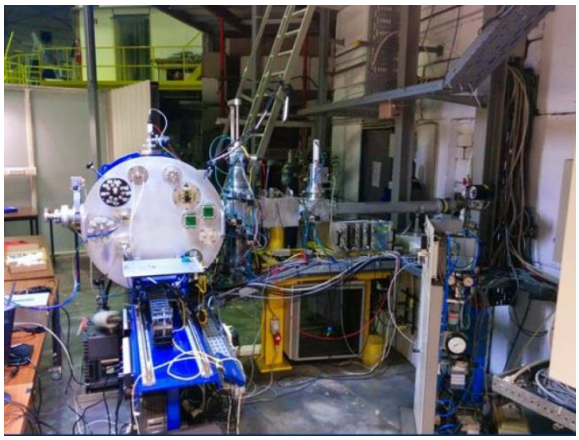

Figure 7 – Ion Beam and Radiation Chamber

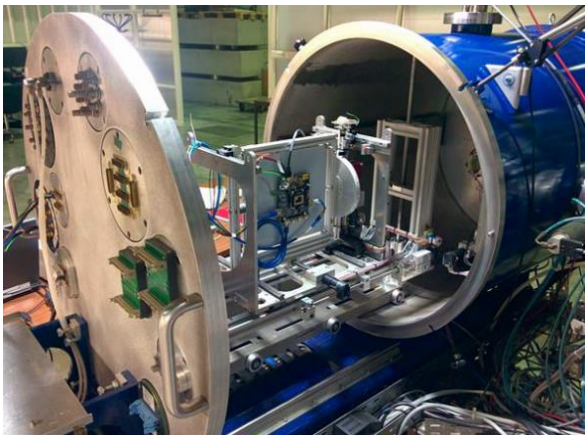

Figure 8 – Radiation Chamber Opened

6 CONCLUSIONS

This is the first time that SpaceFibre has been implemented in a radiation tolerant ASIC. Radiation results show no SEL events although further work is required to clarify the nature of the SEFI events observed. TID tests proved no changes for a dose of 300 kRads. Finally, different set-up testing in the laboratory proved the correct operation of VHiSSI under realistic functional scenarios. The correct operation of SpFi has been assessed in a space qualified device.

7 ACKNOWLEDGMENTS

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