SpaceFibre: The Standard, Simulation, IP Cores and Test Equipment

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ABSTRACT

SpaceFibre is an emerging new standard for spacecraft on-board data-handling networks. Initially targeted to deliver multi-Gbit/s data rates for synthetic aperture radar and high-resolution, multi-spectral imaging instruments, SpaceFibre has developed into a unified network technology that integrates high bandwidth, with low latency, quality of service (QoS) and fault detection, isolation and recovery (FDIR). Furthermore SpaceFibre is backwards compatible with the widely used SpaceWire standard at the network level allowing simple interconnection of existing SpaceWire equipment to a SpaceFibre link or network.

Developed by the University of Dundee for the European Space Agency (ESA) SpaceFibre is able to operate over fibre-optic and electrical cable and supports data rates of 2 Gbit/s in the near future and up to 5 Gbit/s long-term. Multi-laning improves the data-rate further to well over 20 Gbits/s.

This paper details the current state of SpaceFibre which is now in the process of formal standardisation by the European Cooperation for Space Standardization (ECSS). It describes the SpaceFibre IP core being developed for ESA along with the design of an experimental SpaceFibre ASIC. The design of a SpaceFibre demonstration board is introduced and available SpaceFibre test and development equipment is described. The way in which several SpaceWire links can be concentrated over a single SpaceFibre link will be explained.

1 INTRODUCTION

SpaceFibre [1] [2] [3] [4] is a multi-gigabit/s serial network technology being designed specifically for spaceflight applications. SpaceFibre aims to support high data-rate payloads, for example synthetic aperture radar and hyper-spectral optical instruments. It provides robust, long distance communications for launcher applications and supports avionics applications with deterministic delivery capability.

SpaceFibre provides a quality of service mechanism able to support priority, bandwidth reservation and scheduling. It incorporates fault detection, isolation and recovery (FDIR) capability in the interface hardware. It is designed to be implemented efficiently, requiring only three times the number of logic gates of a SpaceWire [5] interface while providing many capabilities missing from SpaceWire.

2 ECSS SPACEFIBRE STANDARD

SpaceFibre is currently a mature draft standard being specified by the University of Dundee with contributions from ESA, JAXA, NASA, Airbus DS, Thales Alenia Space, SubMicron, ELVEES, NEC Toshiba Space, Misubishi Heavy Industries, St Petersburg University of Aerospace Instrumentation, University of Pisa and other organisations. The protocol stack for SpaceFibre is illustrated in Figure 1.

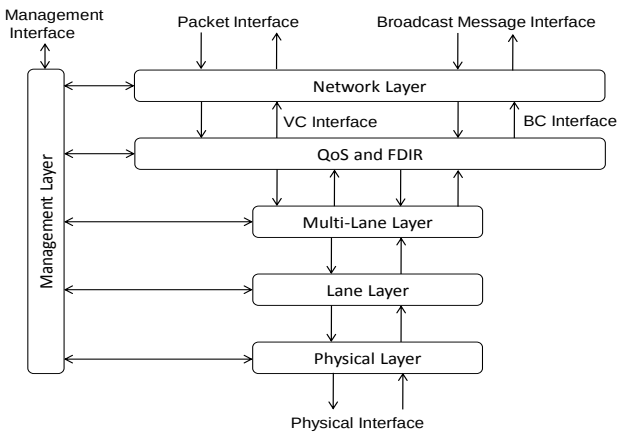

Figure 1 - SpaceFibre Protocol Stack

The network layer protocol provides two services for transferring application information over a SpaceFibre network; the packet transfer service and the broadcast message service. The Packet Transfer Service transfers SpaceFibre packets over the SpaceFibre

network, using the same packet format and routing concepts as SpaceWire. The broadcast message service broadcasts short messages carrying time and synchronisation information to all nodes on the network.

The QoS and FDIR layer provides quality of service and flow control for a SpaceFibre link. It frames the information to be sent over the link to support QoS and scrambles the packet data to reduce electromagnetic emissions. It also provides an error recovery capability; detecting any frames or control codes travelling over a link that go missing or arrive containing errors and resending them.

The Multi-Lane layer is able to operate several SpaceFibre lanes in parallel to provide higher data throughput. In the event of a lane failing the Multi-Lane layer provides support for graceful degradation, automatically spreading the traffic over the remaining working links. It does this rapidly without any external intervention.

The Lane layer initialises each lane and re-initialises any lane that detects an error. Data is encoded into symbols for transmission using 8B/10B encoding and decoded in the receiver. 8B/10B codes are DC balanced supporting AC coupling of SpaceFibre interfaces.

The Physical layer serialises the 8B/10B symbols and sends them over the physical medium. In the receiver the Physical layer recovers the clock and data from the serial bit stream, determines the symbol boundaries and recovers the 8B/10B symbols. Both electrical cables and fibre-optic cables are supported by SpaceFibre.

The management layer supports the configuration, control and monitoring of all the layers in the SpaceFibre protocol stack.

The SpaceFibre standard has been simulated, implemented and reviewed at all stages of its research, design and development. The physical, lane and QoS layers of SpaceFibre are fully defined and have been extensively tested with simulations by at least three independent organisations, and by implementation in FPGAs. The multi-lane layer has been designed and simulated, and is currently in the process of being implemented and tested in FPGAs.

The formal European Cooperation for Space Standardization (ECSS) activity on SpaceWire is scheduled to start in April 2015. The SpaceFibre standard will cover the physical, lane, multilane, QoS and management layers, everything necessary for high-speed point-to-point links. The SpaceFibre network layer will be a separate standard document. The network layer uses the same packet format as SpaceWire and supports path and logical addressing.

3 SPACEFIBRE SIMULATION

As SpaceFibre was being designed by the University of Dundee, various alternative designs were simulated and traded-off with ad hoc software implementations. The aim of this simulation work was to rapidly explore alternative designs rather than provide formal validation of the standard specification.

During the SpaceWire-RT EC Framework 7 project, St. Petersburg University of Aerospace Instrumentation, performed extensive simulation of the SpaceFibre standard using SML to validate the available levels of the SpaceFibre specification and System-C to explore network level attributes of SpaceFibre [6]. Feedback on issues and errors in the SpaceFibre specification was given for drafts C, D and E.

As part of the current ESA SpaceFibre Demonstrator activity Thales Alenia Space France (TAS-F) have developed an OpNet simulation of the SpaceFibre lane and QoS layers and validated their operation and specification in the draft standard specification [7]. The multi-lane layer is scheduled to be simulated in the near future.

4 SPACEFIBRE IP CORE

In parallel with specifying the SpaceFibre standard the University of Dundee and STAR-Dundee designed and tested a VHDL IP core for SpaceFibre. This was necessary to ensure that an implementation of SpaceFibre was efficient in terms of both performance and gate count. The SpaceFibre IP core was implemented in an FPGA to help test and validate the SpaceFibre specification. The IP core was used at all stages of the draft specification to validate and prove the concepts being explored. As a consequence, the VHDL IP core has gone through as many iterations as the SpaceFibre specification. At present the VHDL IP core implements all layers of the SpaceFibre specification with the exception of the Multi-Lane layer. This VHDL IP core is available from STAR-Dundee Ltd [8].

A block diagram showing the interfaces to the IP Core is given in Figure 2. The current version SpaceFibre IP core is compliant to the draft F3 version of the SpaceFibre standard and supports all its features with the exception of multi-laning.

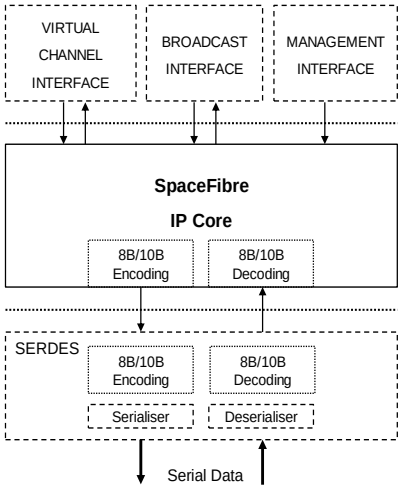

Figure 2 - SpaceFibre IP Core Interfaces

The SpaceFibre IP Core is designed to interface with an external SerDes device using the internal 8B/10B encoder/decoder or to an external 8B/10B encoder/decoder and SerDes device. This allows the SpaceFibre IP Core to be used with space qualified SerDes such as the TLK2711-SP device from Texas Instruments. The application interface to the SpaceFibre IP core comprises three separate interfaces:

1. A virtual channel interface, which is used to send and receive SpaceFibre packets over the virtual channels in the interface.
2. A broadcast interface, which is used to send broadcast messages over the SpaceFibre network.
3. A management interface, which is used to configure, control and monitor the status of the SpaceFibre interface.

The footprints of a SpaceFibre link with a single virtual channel when implemented in various types of space qualified, radiation tolerant FPGAs are listed below:

- Xilinx XQR4VLX200: 5%
- Xilinx XQ5VLX330: 2%
- Microsemi RTAX2000S: 25%.

The utilisation for an 8 virtual channel interface is about twice that of a single virtual channel interface.

5 VHISSI EXPERIMENTAL ASIC

An experimental radiation tolerant SpaceFibre interface device has been developed by University of Dundee, STAR-Dundee, Ramon Chips, ACE-IC, IHP, Airbus DS and SCI within the Very High Speed Serial Interface (VHiSSI) European Commission Framework 7 project [9]. The VHiSSI chip integrates a complete SpaceFibre protocol engine, together with the physical layer interfaces, in a radiation tolerant chip manufactured by a European foundry. A block diagram of The VHiSSI device is shown in Figure 3.

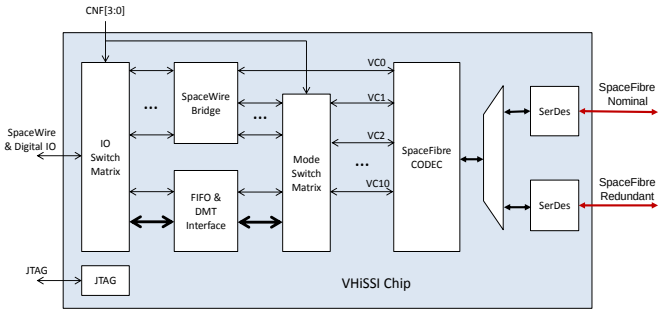

Figure 3 - VHiSSI Chip Block Diagram

There are five main functions within the VHiSSI chip:

- SpaceWire Bridge
- FIFO, DMA, Memory and Transaction Interface
- SpaceFibre Interface
- SerDes
- IO Switch Matrix
- Mode Switch Matrix

The SpaceWire Bridge provides a bridge between SpaceWire and SpaceFibre with up to 11 SpaceWire interfaces being available. The SpaceWire Bridge includes a seven port SpaceWire router which allows routing between three SpaceWire ports, three Virtual Channel (VC) buffers of the two SpaceFibre interfaces and a device configuration port. Configuration of the VHiSSI chip can be carried out over any SpaceWire interface connected to the embedded SpaceWire router or over VC0, VC1 and VC2 of the SpaceFibre interface. The SpaceWire Bridge is connected to the IO Switch Matrix and to the Mode Switch Matrix.

The FIFO and DMA, Memory and Transaction (DMT) Interface provides various types of parallel interface into the VHiSSI chip for sending and receiving data over the SpaceFibre interfaces. The various parallel interface functions have been designed with specific application scenarios in mind and between them are able to operate with many types of local host system, including FPGAs and processors. The parallel interface is also designed to use a small number of pins, so that the VHiSSI chip can fit into a small (100 pin) package

The SpaceFibre Interface has 11 virtual channels. VC 0 is intended primarily for VHiSSI device and local system configuration and monitoring and is connected to the embedded SpaceWire router. VC1 and VC2 are connected to the embedded SpaceWire router. The other VCs are connected directly to a SpaceWire interface, or to the parallel interface, depending on the mode of operation. Each VC supports full SpaceFibre QoS which can be configured independently for each VC.

VC0 is directly connected to the embedded SpaceWire router. The other SpaceFibre VC buffers are

connected to the Mode Switch Matrix which connects them to either the SpaceWire Bridge or the parallel interface. The SpaceFibre interface is connected via a multiplexer to either the nominal or redundant SerDes and CML transceiver.

The SerDes converts parallel data words from the SpaceFibre interface into a serial bit stream and vice versa. On the receive side the bit clock is recovered from the serial bit stream by the SerDes. The SerDes includes integral CML transceivers.

The IO Switch Matrix connects either the SpaceWire LVDS, SpaceWire LVTTL or parallel interface signals from the FIFO and DMT interface to the digital IO pins of the VHiSSI chip. Configuration is static and determined on exit from device reset.

The Mode Switch Matrix connects either the SpaceWire Bridge or FIFO and DMT interface (parallel interface) to the VC buffers of the two SpaceFibre interfaces. Configuration is static and determined on exit from device reset.

The digital logic for VHiSSI was designed by STAR-Dundee Ltd. with system architectural design and project management being carried out by University of Dundee. Airbus DS provided inputs to the VHiSSI requirements. The back end design was carried out by Ramon Chips. ACE-IC designed the SerDes parts of the chip. Test vectors were prepared by STAR-Dundee and SCI with inputs from other partners. The chip was manufactured by IHP. The resulting VHiSSI chip is shown in Figure 4.

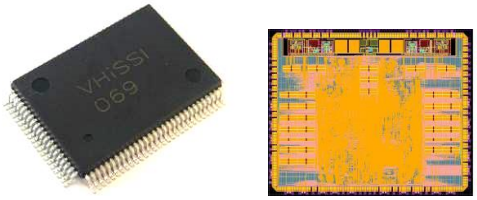

Figure 4 - VHiSSI SpaceFibre Chip

The three major modes of the VHiSSI have been tested in hardware in the laboratory. The board used for testing the SpaceWire LVTTL bridge mode of operation in shown in Figure 5.

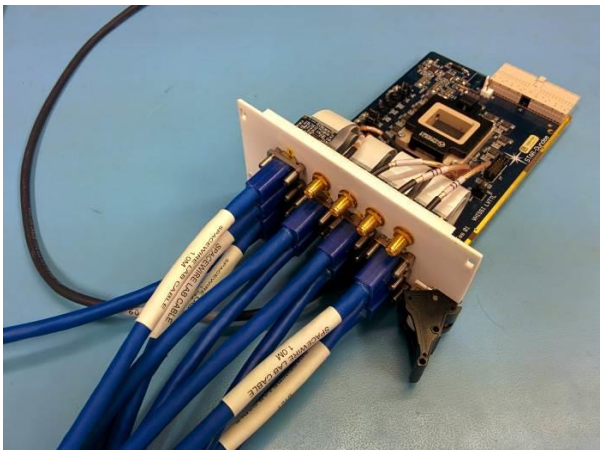

Figure 5 - VHiSSI SpaceFibre to SpaceWire Test Board

The VHiSSI chip is housed in the centre of the board in a specially designed socket, which has a hole in the top to permit Single Event Effect radiation testing of the VHiSSI device. The 11 SpaceWire links are attached to the front panel of the test board (blue cable) and are concentrated by the VHiSSI chip over the SpaceFibre cable (black cable).

The test set up for this board is illustrated in Figure 6. Two eight-port SpaceWire routers are used to connect to all the SpaceWire ports of the VHiSSI chip. A STAR Fire unit is connected to the SpaceFibre cable and also to a host computer, via SpaceWire and a SpaceWire-USB Brick. Software on the host computer was written to exercise and test the function of the VHiSSI chip, providing a test report for each device tested.

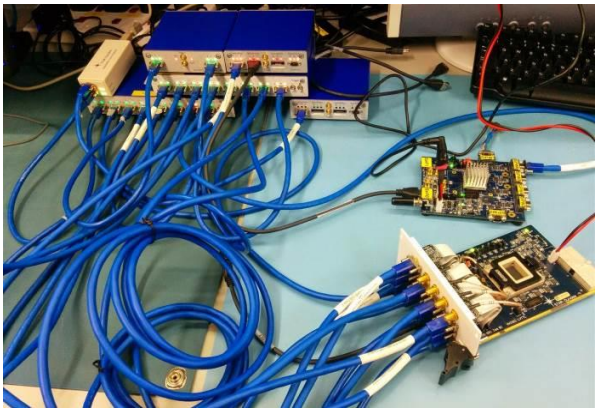

Figure 6 - Test Setup for SpaceWire to SpaceFibre Board

6 SPACEFIBRE DEMONSTRATION BOARD

To raise the TRL of SpaceFibre a spaceflight engineering model is being developed by Airbus DS and ISD in the frame of the ESA SpaceFibre Demonstrator project led by University of Dundee [10]. This uses the Dundee IP core integrated with some other interface and test logic in a Microsemi AX2000

FPGA. Texas Instrument TLK2711 devices are used for the serialisation and de-serialisation. Both devices are available in radiation tolerant, space grade parts. A block diagram of the planned SpaceFibre engineering model is illustrated in Figure 7 Extensive testing, including EMC testing, will be carried out with this board.

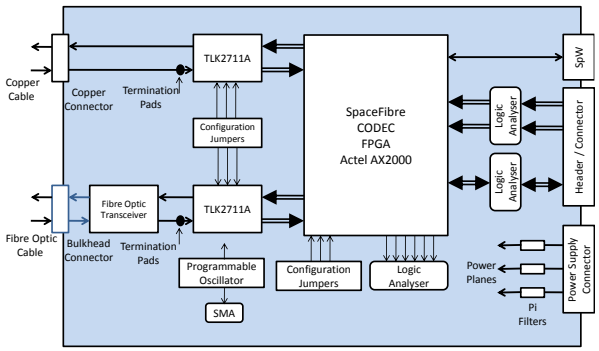

Figure 7 - SpaceFibre Demonstration Board

7 SPACEFIBRE TEST AND DEVELOPMENT EQUIPMENT

7.1 STAR Fire

To support the testing of SpaceFibre a suitable test platform was required, so STAR-Dundee Ltd. developed the STAR Fire unit. A block diagram of this unit is illustrated in Figure 8.

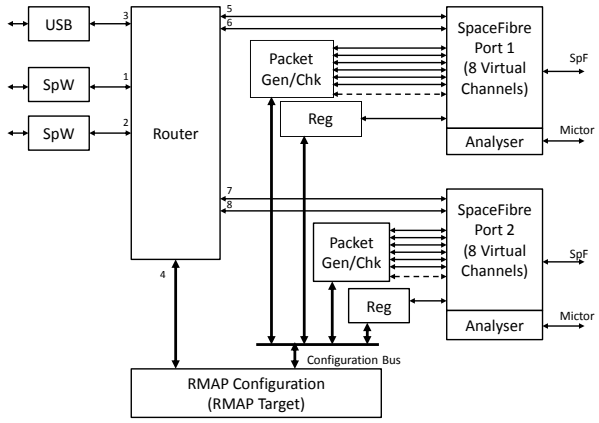

Figure 8 – STAR Fire Unit

The STAR-Fire unit contains two SpaceFibre interface each with eight virtual channels. Two virtual channels of each SpaceFibre interface are connected to a SpaceWire router, which also has two SpaceWire ports, a USB port and an RMAP configuration port. This allows the two SpaceWire interfaces and the USB interface to send packets through either SpaceFibre interface. To test the SpaceFibre interface at full speed and to exercise and validate the bandwidth reservation, priority and scheduled qualities of service, a packet generator and checker is attached to six of the virtual channels of each SpaceFibre interface. The STAR Fire unit is configured and controlled by a Remote Memory Access Protocol (RMAP) interface attached to the SpaceWire router. This allow configuration to be performed over the SpaceWire interfaces, USB interface or the SpaceFibre interfaces. Each SpaceFibre interface has an analyser attached which can be used to record and analyse the operation of the SpaceFibre interface. This was a very important capability during testing of the SpaceFibre IP core and validation of the standard. A graphical user interface provides access to all the capabilities of STAR Fire. An example analysis display is shown in Figure 9.

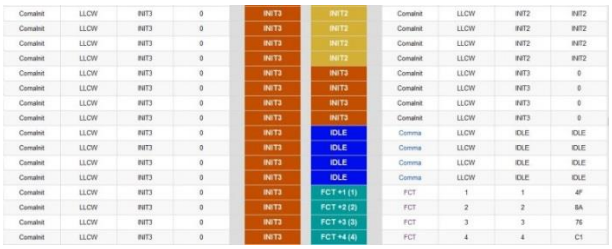

Figure 9 – STAR Fire Analysis Display

7.2 SpaceFibre Lite

The SpaceFibre IP core has been designed to support the testing of the SpaceFibre standard. It has not been designed for speed or size. A version of the SpaceFibre IP core targeted for high performance and small size in flight-qualified FPGAs is currently being developed by STAR-Dundee Ltd. This SpaceFibre Lite IP core is designed to support instrument interfacing with SpaceFibre using existing flight proven FPGAs and SerDes devices. The aim is to be able to implement a complete SpaceFibre interface in significantly less than 20% of an RTAX 2000 FPGA while operating at 2.5 Gbits/s data signalling rate with a TLK2711 SerDes.

An FMC board has been designed by STAR-Dundee containing the SpaceFibre Lite IP core programmed into an AX1000 FPGA device. Connected to a TLK2711 SerDes it provides a complete SpaceFibre interface with one 2 Gbits/s data-rate virtual channel for high-speed instrument data transfer and one slower virtual channel with a SpaceWire Remote Memory Access Protocol (RMAP) interface for instrument configuration and control, and gathering of housekeeping information. The SpaceFibre Lite FMC board may be connected to a commercial FPGA evaluation board for rapid prototyping and evaluation of high data-rate instrument interfaces and other SpaceFibre systems. The SpaceFibre Lite IP core can then be used for spaceflight implementation integrating SpaceFibre and user logic in a single FPGA.

Further information on SpaceFibre Lite will be provided in the full paper.

7.3 SpaceWire to SpaceFibre Bridge

A SpaceWire to SpaceFibre bridge interface board is also available from STAR-Dundee which is similar to the SpaceWire bridge mode of the VHiSSI chip. Implemented on a cPCI/PXI board it provides a bridge between up to 12 SpaceWire ports and a SpaceFibre interface. This can be used to prototype and evaluate the carrying of data from multiple SpaceWire devices over a single SpaceFibre link.

7.4 Other SpaceFibre Test and Development Equipment

The full paper will describe other SpaceFibre test and development equipment which is currently being designed by STAR-Dundee Ltd.

8 CONCLUSIONS

SpaceFibre is now in the process of being adopted as a formal ECSS standard. Providing multi-gigabit/s communications it incorporates a comprehensive quality of service capability providing integrated bandwidth reservation, priority and scheduling. Efficient, effective and rapid fault detection, isolation and recovery mechanisms are included in the SpaceFibre interface, enabling rapid detection and recovery from link level errors.

SpaceFibre has been simulated, implemented and tested extensively in support of the standard specification. Several beta site evaluations of SpaceFibre are underway using the SpaceFibre IP core in various spacecraft applications. Flight connectors and cable for both electrical and fibre-optic media are being developed. A SpaceFibre engineering is currently being developed to raise the TRL of SpaceFibre.

9 ACKNOWLEDGMENTS

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