A Prototype SpaceVPX Lite (VITA 78.1) System using SpaceFibre for Data and Control Planes

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Abstract - **SpaceVPX (VITA78.0) is a new development in the area of standard backplanes for spacecraft applications, which addresses the key issue of fault tolerance. SpaceVPXLite (VITA78.1) is a derivative of SpaceVPX which is aimed at small size. SpaceFibre is the next generation of the widely used SpaceWire on-board network technology. SpaceFibre runs at multi-Gbits/s over both electrical and fibre-optic cables. SpaceFibre is capable of fulfilling a wide range of spacecraft on-board communications applications because of its inbuilt quality of service (QoS) and fault detection, isolation and recovery (FDIR) capabilities. SpaceFibre is being incorporated in the SpaceVPXLite standard as a protocol for sending information over a backplane. STAR-Dundee is developing a demonstration system of SpaceFibre in SpaceVPXLite, using the Microsemi RTG4 radiation tolerant FPGA. This demonstration system is being used as the engineering model of a UK THz radiometer instrument processing unit.**

Index Terms—**SpaceWire, SpaceFibre, Network, SpaceVPX, VITA, Spacecraft On-board Data-Handling, FPGA, RTG4, Radiation Tolerant, Quality of Service, FDIR, Next Generation Interconnect.**

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1. INTRODUCTION

There is a growing need for a standard electronics backplane for spacecraft on-board processing systems to help reduce development costs, timescales and schedule risk, and to increase the reuse of proven components. Standard backplane racks are widely used in commercial, industrial and military applications, but spacecraft electronics tend to be bespoke, owing to the severe environment and mass and size constraints. The primary issue with operation in the space environment is the general lack of serviceability and the resulting need for the system to operate reliably for many years. It must be possible to recover from any single fault on a spacecraft and to prevent a fault from propagating to other parts of the spacecraft systems. SpaceVPX [1] is a new development in the area of standard backplanes for spacecraft applications, which addresses the key issue of fault tolerance. SpaceVPXLite [2] is a derivative of SpaceVPX which is aimed at small size.

SpaceFibre [3][4][5][6] is being designed into the SpaceVPXLite standard as an optional backplane communication medium. SpaceFibre is the new generation of SpaceWire [7][8] technology for spacecraft on-board communication.

This paper first introduces SpaceFibre and SpaceVPXLite. It then explains the role of SpaceFibre in SpaceVPXLite and describes a generic processing system architecture using SpaceFibre and SpaceVPXLite. The design of a

demonstration system for this technology is then introduced. Finally, a specific space instrument application of this technology is described and conclusions presented.

2. SPACEFIBRE

SpaceFibre is a new standard for spacecraft on-board data-handling networks, initially designed to deliver multi-Gbit/s data rates for synthetic aperture radar and high-resolution, multi-spectral imaging instruments. The addition of quality of service (QoS) and fault detection, isolation and recovery (FDIR) capabilities to SpaceFibre has resulted in a unified network technology. SpaceFibre provides high bandwidth, low latency, fault isolation and recovery suitable for space applications, and novel QoS that combines priority, bandwidth reservation and scheduling and which provides babbling node protection. SpaceFibre is backwards compatible with the widely used SpaceWire standard at the network level allowing simple interconnection of existing SpaceWire equipment to a SpaceFibre link or network.

The multi-laning capabilities of the SpaceFibre protocol [9] allow several lanes to operate in parallel to provide enhanced throughput [10]. For example, with four lanes each running at 2.5 Gbits/s an aggregate throughput of 10 Gbits/s is achieved. SpaceFibre multi-laning can operate with any number of lanes, from 1 to 16. Each lane is normally bi-directional, but to support spaceflight instruments with very high-data rate in one direction and to save mass and power, it is possible to have some uni-directional lanes in a multi-lane link, provided that at least one lane is bi-directional. SpaceFibre multi-laning also supports graceful degradation in the event of a lane failure. If a lane fails, the multi-lane link will rapidly reconfigure to use the remaining lanes so that important (high priority) information can still get through. It takes a couple of microseconds for this reconfiguration to occur, which happens without loss of information. Clearly, with reduced bandwidth some information will not be sent over the link, but this will be less important, low priority, information. If a redundant lane is available in the link, it can be enabled and full capacity operation will resume.

3. VITA 78.1 SPACEVPXLITE

VITA is an organisation that defines computer bus, board, and system specifications such as VMEbus, PMC and FMC. Switched serial technologies offer significant benefits over parallel interconnect technologies including: higher bandwidth; lower latency; reduced contention; improved scalability and reduced footprint. To take advantage of this VITA defined the VPX series of standards (VITA 46.0) [10] which provide a standard mechanical format to support the standardisation of switched serial interconnects for applications in rugged environments. VPX sacrifices interoperability in favour of flexibility, allowing many possible serial interconnects to be used as the data plane. Users can select their preferred serial technology, but one implementation is not guaranteed to be interoperable with another.

SpaceVPX (VITA 78.0) [1] takes the ruggedized VPX standard one step further, addressing the need for redundancy in spaceflight systems and focussing on conduction cooled racks. SpaceVPX replaced the VMEbus control-plane of VPX with SpaceWire, but retained the versatility of a user defined data plane serial interconnect. SpaceVPX concentrates on meeting a wide range of applications and in defining sets of “backplane profiles” to support those applications, rather than defining a common interconnect interface. This approach makes the SpaceVPX standard very complex, because it includes so many options, but it is very flexible. SpaceVPXLite (VITA 78.1) [2] aims to reduce the size and complexity of SpaceVPX. It focuses on 3U sized boards, restricts and rationalizes the possible backplane configurations of SpaceVPX and concentrates on the support of utility, control and data planes. The VITA 78.1 standard is currently in draft form.

SpaceVPXLite has four types of module or board that plug into a backplane or rack:

1. System controller module, which controls the operation of the other modules in the rack. There are two system controller modules, one nominal and one redundant. They are connected using radial data connections to the payload modules and using I2C or other “utility” signals to the power supply and power switch modules. The term “radial” is used because these point-to-point connections radiate outwards from the system controller to the payload modules.

2. Payload module, which is the main processing or data-handling functions. There are a maximum of six payload modules in the rack. Redundancy of the payload modules can be arranged according to the application requirements. For example, if the payload modules all provide the same type of function they might be arranged as five operational and one redundant unit.

3. Power supply module, which provides power to the power switch modules for distribution to the other modules in the rack. There are two power supply modules, nominal and redundant. The input supply voltage is typically 24 Volt DC.

4. Power switch module, which distributes power from the nominal or redundant power supply to the system controller and payload modules. The power to the system controllers is switched depending on some external signals and the power to the payload modules is selected by the active system controller according to current mission requirements. The power switch module includes redundancy of the control circuitry, which is used according to which system controller is currently active.

SpaceVPXLite separates the backplane communications into three principal planes or functions:

1. Control plane, which is used to pass configuration, control and monitoring information between the system controllers and the payload modules. It is possible to pass data for processing by the system controller between the system controller and the payload boards. The control plane is normally implemented with independent SpaceWire links running from each system controller to each payload module. That is a total of six links from each system controller and two links (nominal and redundant) into each payload module.

2. Data plane, which is used to pass information between the payload modules. Data typically arrives from a sensor via one or more front panel connectors on a payload board and is distributed as required via the backplane between the payload boards for processing, compression, storage, etc. The data plane supports several possible multi-Gbits/s serial technologies, for example Serial Rapid IO. Both switch and point-to-point connections can be used to interconnect the payload modules.

3. Utility plane, which is used to pass power, clock signals and control/status signals between the various modules in the SpaceVPXLite rack.

An example SpaceVPXLite backplane is illustrated in Figure 1.

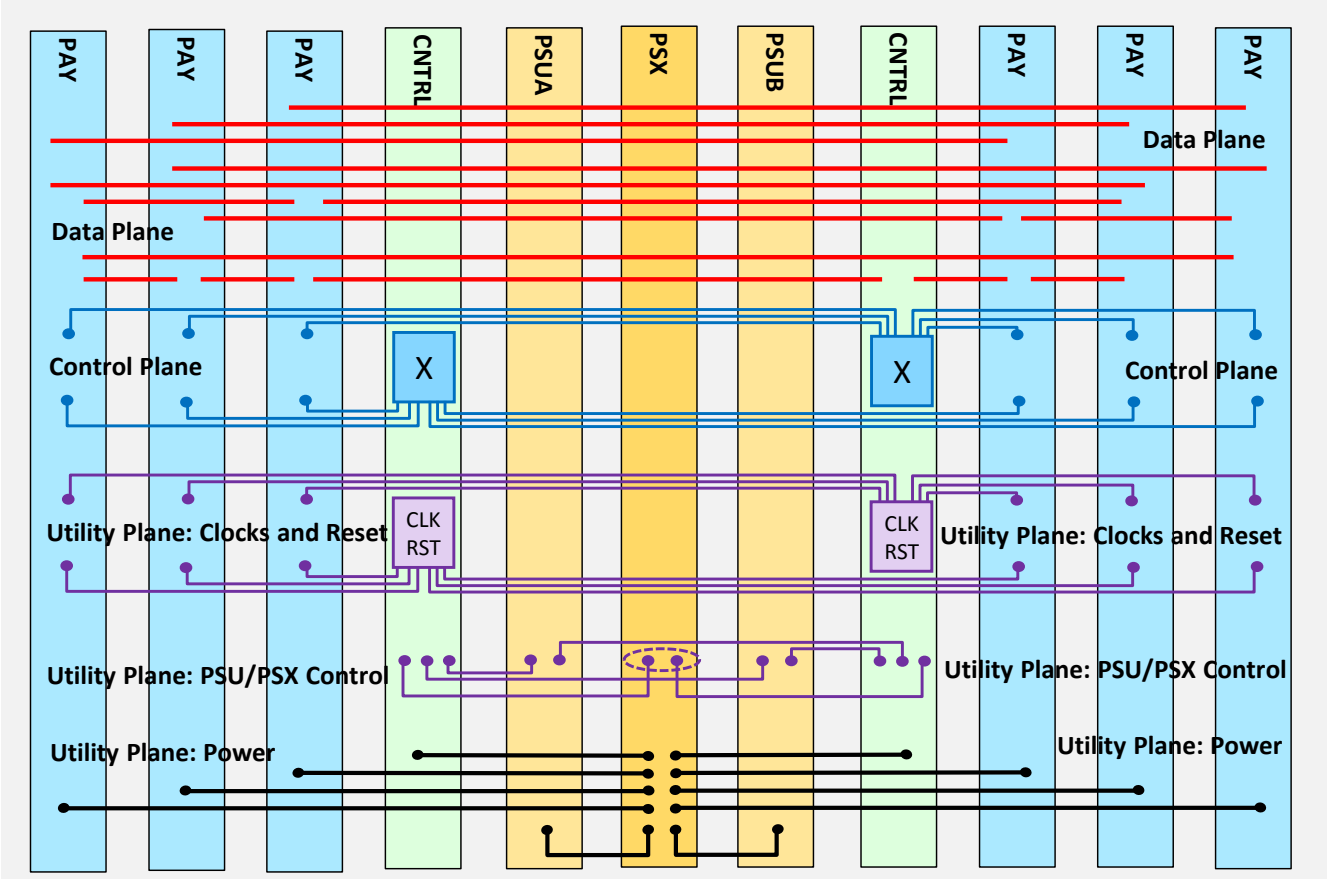

Figure 1 Backplane Connections

There are two power supplies, nominal and redundant, with power switches (which can be integrated on the same board), two system controller boards, nominal and redundant, and up to six payload boards, which can be processors, mass memory modules or other functions. The power switches distribute power to the active boards. A combined control, data and system management plane interconnects the controllers and the payload modules. Other utility functions like clock distribution, are carried by specific utility signals. In this example the main power used by the system controller and payload modules is 5 Volt, so only one power switch is used. If 3.3 Volt or 12 Volt power is required, additional power switch modules would be required.

The control plane is responsible for configuration, control and monitoring of the payload modules by the active system

controller. The data plane provides high-bandwidth communication between payload modules.

4. SPACEFIBRE SUPPORT IN SPACEVPXLITE

SpaceFibre can fulfil various roles in a SpaceVPXLite system, which are discussed in this section.

SpaceFibre as the Data Plane

SpaceFibre can be used as the data plane in a SpaceVPXLite system because it is fully compatible with the 100 ohm differential impedance backplane connections provided for the data plane. A SpaceFibre interface with up to four lanes can be used to provide data rates of up to 12.5 Gbits/s (10 Gbits/s data throughput) with current radiation tolerant implementations. The principal advantages of using SpaceFibre compared to Serial Rapid IO for the data plane are:

- Graceful degradation: SpaceFibre multi-lane operation provides graceful degradation in the event of a lane failure. Around 2 μs after the fault has been detected the link continues operation with the remaining lanes. For example, if there are four lanes and one fails, the link carries on using the remaining three lanes. The subsequent loss of bandwidth is handled by the inbuilt QoS within SpaceFibre. The important, high-priority information will use the available bandwidth; data with low priority will not be transferred. By assigning appropriate priority levels and allocating appropriate reserved bandwidths to each of the virtual channels on a SpaceFibre link, the user can determine the traffic profile both during normal operation and when a fault occurs in a lane.

- Quality of Service: SpaceFibre provides an innovative quality of service mechanism that combines priority, bandwidth reservation and scheduling. This allows deterministic data delivery without wasting network bandwidth. SpaceFibre also provides a low latency broadcast message service, which is able to distribute time and synchronisation information rapidly to all nodes on the SpaceFibre network.

- Footprint: SpaceFibre has been design to have a substantially smaller footprint than Serial Rapid IO. This means that it is possible to integrate many SpaceFibre interfaces in an FPGA such as the Microsemi RTG4 FPGA.

SpaceFibre as the Control Plane

SpaceVPX and SpaceVPXLite uses SpaceWire as a control plane. SpaceWire is widely used in space applications, supports moderate data rates and has a small footprint. There are two disadvantages of using SpaceWire: lack of AC coupling which requires special cold sparing interfaces and the fact that a SpaceWire interface requires eight signal wires. SpaceFibre has been designed to be backwards compatible with SpaceWire at the network level. This means that SpaceWire and SpaceFibre share the same packet formats and addressing scheme. To connect between SpaceWire and SpaceFibre is thus trivial, simply connecting a SpaceWire interface to a SpaceFibre virtual channel is all that is required. A SpaceWire unit connected to a SpaceFibre network does not know that it is connected to SpaceFibre, but it benefits from the additional FDIR and QoS capabilities of SpaceFibre.

What this means for SpaceVPXLite is that it is possible to replace a SpaceWire based control plane with a SpaceFibre control plane in a SpaceVPXLite system, without having to change the application software. Two lanes of SpaceFibre can be run over the same number of backplane signals as a SpaceWire link. This results in 6.25 Gbits/s data signalling rate and graceful degradation of the control plane connection. If one SpaceFibre lane fails, the other one keeps going, transferring the critical control information. The SpaceFibre virtual networks allow different classes of traffic to be sent over independent virtual networks, allowing control information to be sent over one virtual network, possible management information over another, and application data over other virtual networks. Essential separation of control information is maintained via the virtual networks and control information can be given high priority, as well as a reserved bandwidth allocation to ensure that this critical information is delivered in the event of a lane failure in a multi-lane link.

Payload Management Function Over the Control Plane

The control plane goes to all of the payload modules from each of the system controllers. This means that there is no need for utility plane signals to carry the system management information. Normally passed over an I2C bus, the system management information can be sent over SpaceWire or SpaceFibre using the Remote Memory Access Protocol [11] to access the management control and status register in the payload boards. When this is done with SpaceFibre, a separate virtual network can be allocated to the system management function. This means that the two I2C buses that would normally run one from each system controller to all of the payload modules are replaced by radial point-to-point connections, which is much better from the redundancy perspective.

5. GENERIC SPACEFIBRE BACKPLANE

The SpaceFibre based backplane for SpaceVPXLite will now be described. Note that this backplane arrangement could be used for other serial protocols, but SpaceFibre is preferred for the reasons outlined previously. Also, other backplane topologies are possible, but the one described is a compromise between providing high-performance interconnect and flexibility.

Figure 2 shows the two system controllers (rectangles) and the six payload modules (circles). Each system controller is connected to every payload module using radial point-to-point connections. These control plane connections could each be either a single SpaceWire link or a two-lane SpaceFibre link.

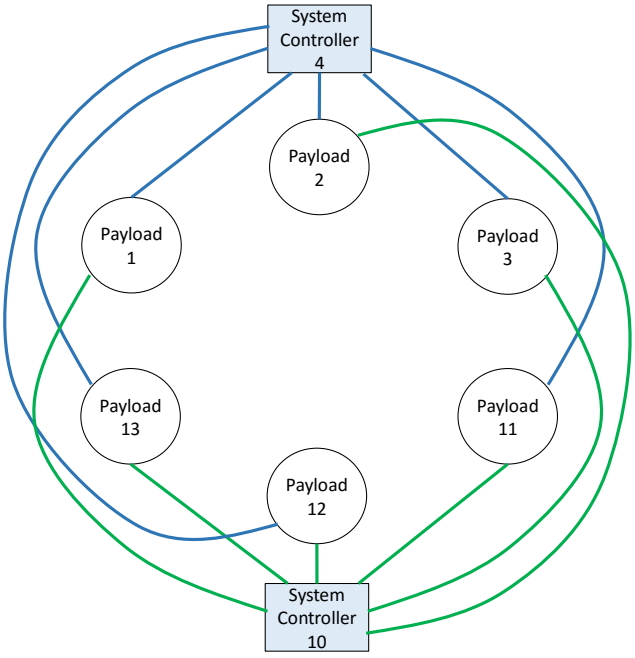

Figure 2 Nominal and Redundant Control Plane Connections from Systems Controllers to Payload Boards

To provide data interconnection between the six payload modules a fully connected mesh structure is employed with each payload module connected by a four-lane SpaceFibre link to every other payload module. This is illustrated in Figure 3 by the solid and dashed straight black lines. With a fully connected mesh on the backplane it is possible for an application to implement a ring, dual-ring, full-mesh or various other network topologies between the payload modules. In the diagram the numbers attached to each end of a line are the SpaceFibre interface numbers. For example, the connection between payload 1 and payload 2 connects SpaceFibre interfaces 5-8 on payload 1 to interfaces 1-4 on payload 2.

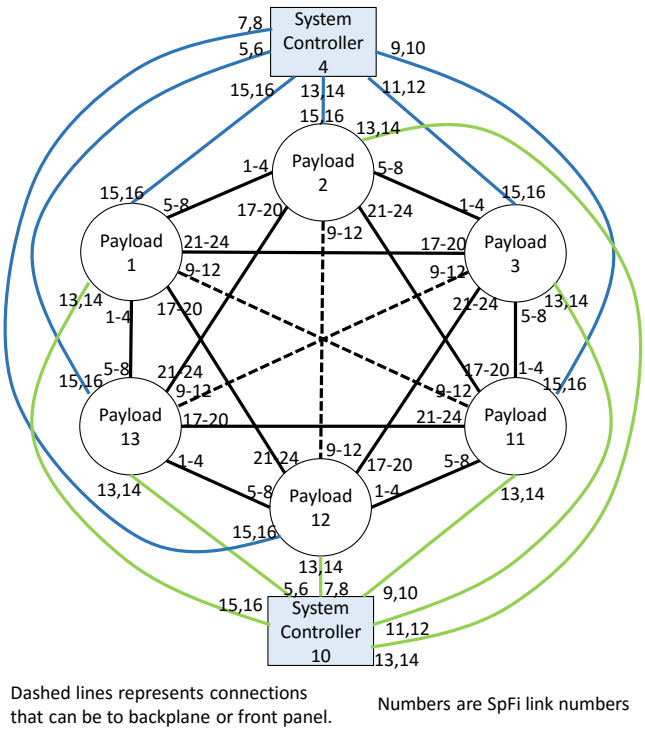

Figure 3 Control and Data Plane Connections

The corresponding backplane architecture for the control and data plane connections is shown in Figure 1.

6. DEMONSTRATION SYSTEM

A demonstration system for SpaceFibre in SpaceVPXLite is being developed by STAR-Dundee with funding from the UK Space Agency. Each of the components of the system will now be described.

SpaceVPX-RTG4 board

The main board being used in the demonstration system is the STAR-Dundee SpaceVPX-RTG4 board. A block diagram of this board is shown in Figure 4 along with a CAD model in Figure 5

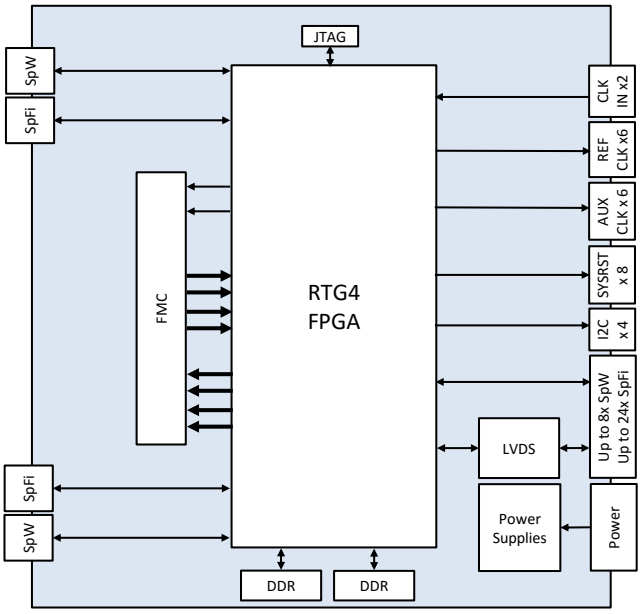

Figure 4 SpaceVPX-RTG4 Board Block Diagram

The main component on the SpaceVPX-RTG4 board is a Microsemi RTG4 FPGA [12][13]. The Microsemi RTG4 is a new generation radiation tolerant FPGA. It has extensive logic, memory, DSP blocks, and IO capabilities and is inherently radiation tolerant, having triple mode redundancy built in. The RTG4 has a flash configuration memory built into the device. In addition the FPGA incorporates 16 SpaceWire clock-data recovery circuits and 24 multi-Gbits/s SerDes lanes to support high-speed serial protocols like SpaceFibre.

The RTG4 can be configured as either a system controller or a payload processor. It provides the following sets of signals to the SpaceVPXLite backplane:

- Power connections from the power switch module.
- Control plane comprising either six SpaceWire links or six, four-lane SpaceFibre links.
- I2C buses to the two power supplies and power switch, used for control and status monitoring of these boards.
- Eight system reset signals, which fan out radially to the six payload processors and to the power supply and switch board.
- Six reference clocks, which are sent radially to the payload processors.
- Six auxiliary clock (synchronisation or periodic pulse signals), which are also sent radially to the payload processors.
- A pair of clock inputs, which are used to derive the clock output signals when the board is acting as a system controller and which provide the nominal and redundant clock inputs when operating as a payload module.

Attached to the RTG4 are two banks of 32-bit wide DDR memory each with 8-bit EDAC parity. A pair of SpaceWire and a pair of SpaceFibre connectors are provided on the front panel of the SpaceVPX-RTG4 board. To provide additional input/output functions an FMC connector is provided on the board. Several FMC boards are being designed to operate with the SpaceVPX-RTG4 board including a 3 Gsamples/s, dual ADC board.

The SpaceVPX-RTG4 board is a conduction cooled, 0.8 inch wide, 3U high board. It is designed where possible using commercial equivalents of flight qualified parts. The board is designed following ESA flight board design guidelines.

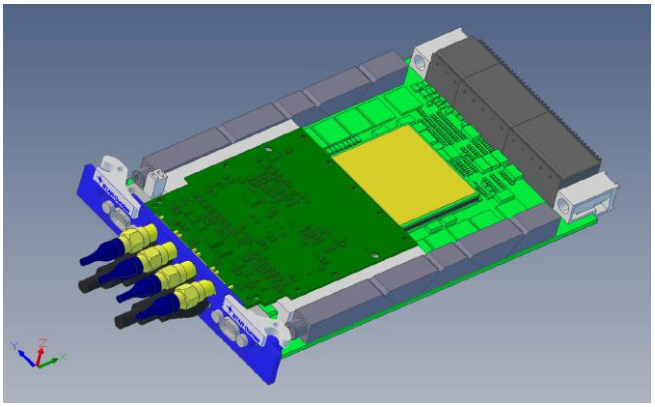

Figure 5 SpaceVPX-RTG4 Board CAD Model with FMC Card Fitted

System Controller

The SpaceVPX-RTG4 board can be configured as a system controller. An ARM Cortex M1 processor is being implemented in the FPGA to provide the necessary control functions. In this configuration the board provides the radial system reset, reference clock and auxiliary clock signals as well as the radial SpaceWire or SpaceFibre control plane signals. Up to four I2C buses are provided for control and monitoring of the power supplies and power switches.

Payload Processor

The SpaceVPX-RTG board can also be configured as a payload processor board. In this case two of the control plane links are used for the connection to the system controllers. The other SpaceWire or SpaceFibre links can be used to provide the data plane connection to other payload processor boards.

Power Switch

The power switch takes 5 Volt and 3.3 Volt power from either the nominal or redundant power unit and switches that power to the system controller boards and the payload boards. The active system controller board is determined by two external control signals. The active system controller board then

controls the power switch board to switch power to the various payload boards as required by the application. A 12 Volt supply is provided to the power switch board which is used to power the control and switch circuitry on the board.

Power Supply

The power supply module provides the following supply voltages:

- 5 Volt main power
- 3.3 Volt auxiliary power
- 12 Volt power for the power switch board

Backplane and Rack

The backplane connections used in the demonstration system are illustrated in Figure 1. The SpaceFibre data plane connections provide the full mesh topology illustrated in Figure 3. The SpaceWire or SpaceFibre control plane runs radially from the two control processors to each payload board. Similarly the utility plane system reset, reference clock and auxiliary clock signals run radially from the system controllers to the payload modules. Utility plane I2C buses run from the system controller to the power supply and power switch modules. Power is distributed from the power switch module to the system controller and payload modules.

7. DEMONSTRATION APPLICATION

The SpaceVPXLite demonstration system is being used to develop the engineering model of the LOCUS THz radiometer [14] being developed by RAL, UCL, University of Leeds, STAR-Dundee and other partners in the UK. STAR-Dundee is responsible for the design of the backend spectrometer. The SpaceVPXLite demonstration system provides up to six payload modules each of which is configured as an FFT processor that processes a 2 GHz wide signal into bins of a few MHz bandwidth. Six of these boards is able to process a total of 12 GHz signal bandwidth.

A block diagram of the SpaceVPX-RTG4 board, configured with a 3 Gsample/s dual ADC, is illustrated in Figure 6. This board takes the 2 GHz bandwidth analogue signal, converts it into a digital signal, performs the FFT and integrates the results to extract the required signal from instrument noise.

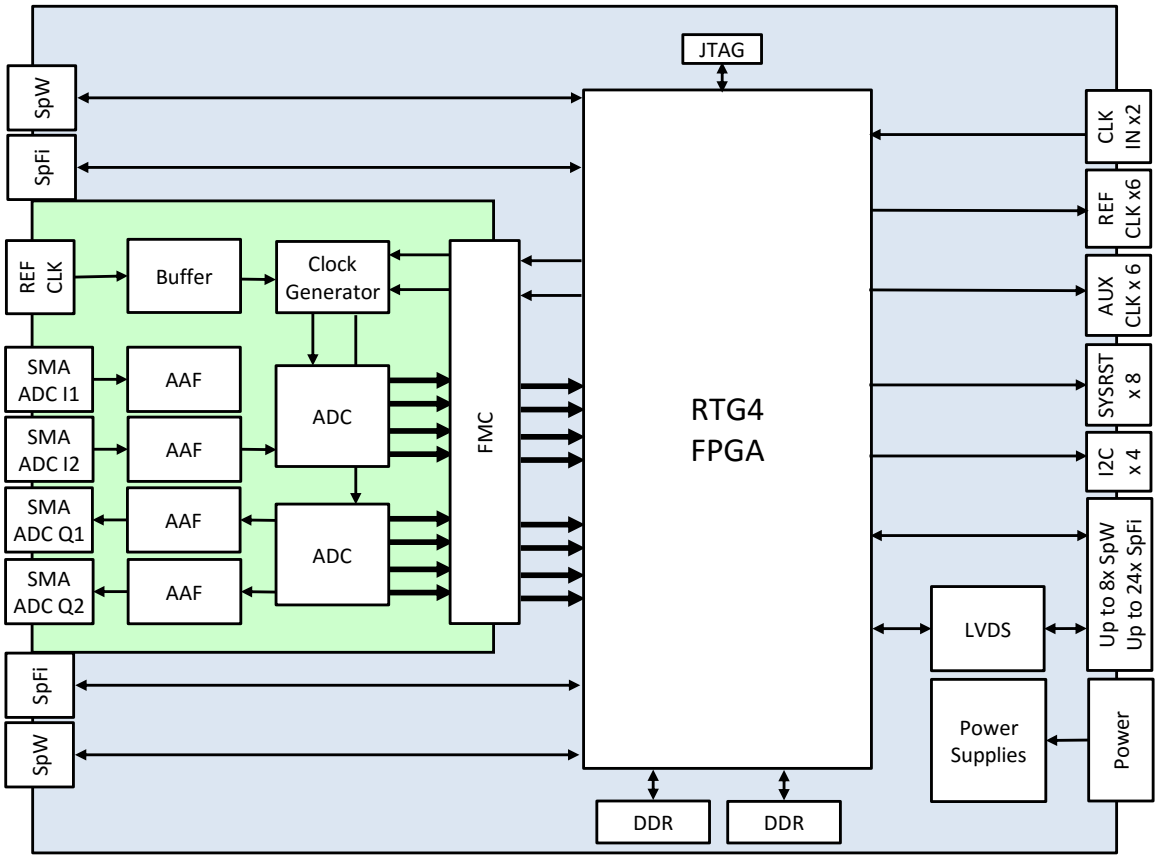

Figure 6 SpaceVPX-RTG4 Board Block Diagram with Dual ADC FMC Card

The integrated signals from the six FFT processors are passed via the control plane to the system controller. The system controller collates this information and passes the results over one of its two front panel SpaceWire interfaces to the spacecraft data-handling system. The system controller is also used to configure, control and monitor the operation of the FFT processors. Integration and testing of this experimental system is expected in the first half of 2017.

8. CONCLUSIONS

SpaceVPXLite offers the possibility of a standard backplane for space-based instrument processing and payload data-handling applications. This would help reduce development costs, timescales and schedule risk, and increase the reuse of proven components. SpaceFibre is the next generation of SpaceWire on-board data-handling network technology for space applications which is now being developed as a backplane interconnect protocol for SpaceVPXLite. STAR-Dundee is building a demonstration system to prove this technology. The demonstration system is being used as the engineering model of the instrument processing unit for a UK THz radiometer.

The path to acceptance of such a standard, in a domain that often uses bespoke solutions, is not straightforward. SpaceVPXLite must provide the essentials: adequate performance, redundancy and conduction cooling. It must also be close to the mass, size and power consumption of a bespoke solution and it must support reuse, i.e. efficient designs that can be used across multiple missions. The essentials are designed into SpaceVPXLite and work is now focused on the latter requirements, which can really only be proved by building systems for missions. STAR-Dundee is using SpaceVPXLite as the backplane standard for the LOCUS spectrometer with the aim of demonstrating that SpaceVPXLite can be used successfully for spaceflight applications and where there are issues, identifying and understanding them.

ACKNOWLEDGMENTS

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REFERENCES

[1] VITA, "SpaceVPX System", ANSI/VITA 78.00-2015, April 2015.

[2] Scott Goedeke, et al, "SpaceVPX Lite, Lightweight SpaceVPX Systems Specification", VITA 78.1, Draft revision 2.3, VITA, 14 July 2016.

[3] S. Parkes, A. Ferrer Florit and A. Gonzalez Villafranca, "SpaceFibre Standard", Draft H5, University of Dundee, July 2016.

[4] S. Parkes, C. McClements and M. Suess, "SpaceFibre", International SpaceWire Conference, St Petersburg, Russia, 2010, ISBN 978-0-9557196-2-2, pp 41-45.

[5] S. Parkes, A. Ferrer, A. Gonzalez, & C. McClements, "SpaceFibre: Multiple Gbits/s Network Technology with QoS, FDIR and SpaceWire Packet Transfer Capabilities", International SpaceWire Conference, Gothenburg, June 2013.

[6] S. Parkes et al, "SpaceFibre: Multi-Gigabit/s Interconnect for Spacecraft On-board Data Handling", IEEE Aerospace Conference, Big Sky, Montana, 2015.

[7] ECSS Standard ECSS-E-ST-50-12C, "SpaceWire, Links, Nodes, Routers and Networks", Issue 1, European Cooperation for Space Data Standardization, July 2008, available from http://www.ecss.nl.

[8] S. Parkes, "SpaceWire User's Guide", ISBN: 978-0-9573408-0-0, STAR-Dundee, 2012, available from https://www.star-dundee.com/knowledge-base/spacewire-users-guide https://www.star-dundee.com/knowledge-base/spacewire-users-guide (last visited 20th Oct 2016).

[9] A. Ferrer Florit, A. Gonzalez Villafranca and S. Parkes, "SpaceFibre Multi-Lane", International SpaceWire Conference, Yokohama, Japan, 2016, ISBN 978-0-9954530-0-5.

[10] VITA, "VPX Baseline Standard", ANSI/VITA 46.0-2007 (R2013), May 2013.

[11] ECSS Standard ECSS-E-ST-50-52C, "SpaceWire – Remote memory access protocol", Issue 1, European Cooperation for Space Data Standardization, 5 February 2010, available from http://www.ecss.nl.

[12] Microsemi, "RTG4 FPGAs - High-Speed RT FPGAs for Signal Processing Applications", http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtg4 (last visited 20th Oct 2016).

[13] S. Parkes et al, "SpaceWire and SpaceFibre on the Microsemi RTG4 FPGA", IEEE Aerospace Conference, Big Sky, Montana, 2016.

[14] S.P. Rea, et al, "The Low-Cost Upper-Atmosphere Sounder (LOCUS)", 26th International Symposium on Space Terahertz Technology, Cambridge, MA, 16-18 March 2015.

BIOGRAPHIES

Steve Parkes *is the Director of the Space Technology Centre at the University of Dundee leading research on spacecraft on-board data-handling networks (SpaceWire and SpaceFibre), planet surface simulation, autonomous lander navigation, and digital signal and image processing for satellites. Steve wrote the ECSS-E-ST-50-12C SpaceWire standard with inputs from international spacecraft engineers, a technology that is now being used on more than 100 spacecraft. He is currently researching deterministic SpaceWire networks for integrated avionics and payload networks, SpaceFibre a multi-Gbit/s network*

technology for spaceflight applications, vision-based navigation for planetary landers, and FFT based spectrometers for an atmospheric chemistry instrument.

***Albert Ferrer-Florit** has a PhD in high-speed interconnection networks for space applications awarded by the University of Dundee. His PhD research was funded by ESA's Networking/Partnering Initiative after he worked in the on-board data processing group (TEC-EDP) in ESTEC. He is specialised in SpaceWire and SpaceFibre networks, being one of the key developers of the SpaceFibre standard. He started his career at CERN in the Summer Student Programme and is currently working for STAR-Dundee Ltd as a Network and Systems Engineer.*

***Alberto Gonzalez Villafranca** holds a doctorate in data compression for space applications and has been connected to the space field his entire professional career. Alberto has been deeply involved in the definition and implementation of SpaceFibre since he joined STAR-Dundee Ltd. Before working with SpaceFibre he had collaborated with the Gaia mission and worked on a hardware implementation of a deterministic variant of the SpaceWire protocol at the European Space Agency.*

***Chris McClements** is lead chip designer at STAR-Dundee Ltd. He worked at the University of Dundee from 2003 to 2016, where he was responsible for the RTL-level design of the SpaceWire 10X router (Atmel AT7910E). This radiation tolerant ASIC is being used in many ESA missions including the BepiColombo and Solar Orbiter missions. During this time Dr McClements was also the author and developer of the SpaceWire-B and SpaceWire RMAP VHDL IP cores which are available through the ESA IP core service. The SpaceWire IP core is the most widely used IP core in the ESA portfolio and used in many ESA missions employing FPGA and ASIC devices. He is currently working on test and development equipment for high speed serial SpaceFibre devices.*

***Ashish Srivastava** is pursuing PhD on high speed spacecraft data systems, as a research student in Space Technology Centre, University of Dundee. He received Bachelor of Engineering (BE) in Electronics & Communication from Karnataka University, Dharwad, India in 1999. After graduation he joined as Scientist/Engineer in the same year in Indian Space Research Organization (ISRO) and contributed towards the development of Payload Electronics for Indian Remote Sensing Satellites (IRS). He received his Post Graduation in Software Systems from Birla Institute of Science & Technology (BITS) in 2012. As team member and Project Manager, He has worked in Resourcesat and Cartosat Series of Indian Satellites. He is specialized in Analog and Digital electronics systems for spacecraft. His area of interest is in designing of precision, reliable and miniaturized electronics for payloads and its data handling system. He has received 'Young Scientist Award-2008' conferred by Astronautical Society of India and has 9 papers to his credit.*