SpaceFibre Image Sensor and Data Processing Units

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ABSTRACT

The latest and next generations of spacecraft synthetic aperture radar and high-resolution image instruments will provide very high data-rates on-board a spacecraft, in excess of 10 Gbps. SpaceFibre is the next generation of SpaceWire network technology for spacecraft on-board data-handling. It runs over electrical or fibre-optic cables, operates at very high data rates, and provides in-built quality of service (QoS) and fault detection, isolation and recovery (FDIR) capabilities. This paper describes three SpaceFibre based units: an image sensor, an FPGA based processor and a many-core DSP processor. Equipped with SpaceFibre interfaces they demonstrate the ease with which SpaceFibre can be deployed on future space missions.

1 INTRODUCTION

SpaceFibre [1-4] is a new generation of SpaceWire [5-6] technology which is able to support the very high data-rates required by sensors like SAR and multi-spectral imagers. Data rates of up to 25 Gbps are required to support several sensors currently being planned. In addition, a mass-memory unit requires high performance networking to interconnect many memory modules.

To support the development of spaceflight equipment incorporating SpaceFibre, STAR-Dundee has developed a range of SpaceFibre IP cores and SpaceFibre test and development equipment. The IP cores are being used in radiation tolerant FPGA and ASICs. Recently STAR-Dundee has designed a SpaceFibre camera and a SpaceVPX based processing board to demonstrate the ease with which SpaceFibre can be integrated into spaceflight systems and the substantial advantages it can bring.

This paper first introduces SpaceFibre. It then describes the SpaceFibre camera, the SpaceVPX-RTG4 FPGA based processing board and the RC64 many core DSP processor.

2 SPACEFIBRE

SpaceFibre is designed to support high data-rate payloads, including synthetic aperture radar and hyper-spectral optical instruments. It provides robust, long distance communications for launcher applications and supports avionics applications with deterministic delivery constraints through the use of virtual channels. SpaceFibre enables a common on-board network to be used across many different mission applications resulting in cost reduction and design reusability.

SpaceFibre runs over both electrical and fibre-optic media and provides 3.125 Gbps data rate in current radiation tolerant FPGA technology. Higher data rates of 6.25 Gbps data rate per lane are possible with 65nm ASIC technology. SpaceFibre provides a quality of service mechanism which is able to support priority, bandwidth reservation and scheduling. It incorporates fault detection, isolation and recovery (FDIR) capability in the interface hardware. SpaceFibre is designed to be implemented efficiently and has a much smaller footprint than competing technologies such as Serial Rapid IO, taking 3-5% of a Microsemi radiation tolerant RTG4 FPGA [7] which allows plenty of room for the application specific logic.

Several SpaceFibre lanes can be operated in parallel (multi-laning) to give higher data rates or increased reliability. A multi-lane link can have any number of lanes from 1 to 16. Multi-lane operation provides hot redundancy and graceful degradation in the event of a lane failure, simplifying redundancy approaches and maintaining essential communication services over the remaining operational lanes. When a lane fault does occur, recovery is very fast, taking a few µs. SpaceFibre also supports asymmetric links where some of the lanes can be uni-directional. This is particularly useful for high data-rate instruments where data flow is

mainly in one direction, and can save both power and mass.

SpaceFibre is backwards compatible with SpaceWire at the network level, using the same packet format, which allows simple interconnection of existing SpaceWire equipment to a SpaceFibre link or network.

SpaceFibre has a message broadcast capability, which carry eight bytes of user information, together with a broadcast type and channel identifier. This permits, for example, CCSDS unsegmented time information to be broadcast across the spacecraft in a single broadcast message, with low latency. Broadcast messages can be used for time distribution, synchronisation, event signalling, network control and error handling.

The ECSS-E-ST-50-11C SpaceFibre standard will be published in 2018.

STAR-Dundee has developed a comprehensive set of IP cores for SpaceFibre which are already being used in their first space missions and ASIC designs. Both single-lane and multi-lane IP cores are available. In addition, STAR-Dundee has a prototype SpaceFibre router design running on radiation tolerant FPGAs. The following IP cores are now available from STAR-Dundee targeted for Microsemi RTG4 and Xilinx FPGAs, and ASIC implementation:

- Single-lane interface;
- Multi-lane interface;
- SpaceWire to SpaceFibre bridge;
- Routing switch.

3 SPACEFIBRE INSTRUMENTS

STAR-Dundee has developed two prototype instruments with SpaceFibre interfaces: the SpaceFibre camera and the wideband spectrometer. The wideband spectrometer is the subject of a separate paper [8]. The SpaceFibre camera provides a high-resolution, high frame-rate camera which is suitable for both Earth Observation, vision-based navigation and robotic applications. It incorporates a Microsemi RTG4 FPGA which, as well as providing the image sensor interface, control logic and SpaceFibre interfaces, has plenty of room left for data compression or other image processing applications to be integrated in the camera. One specific example is image feature extraction and tracking for the vision-based navigation of planetary landers.

A block diagram of the SpaceFibre Camera is provided in Figure 1.

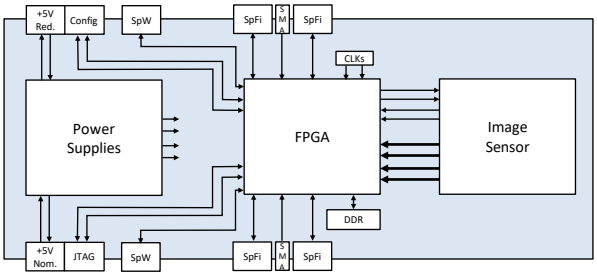

Figure 1: SpaceFibre Camera Block Diagram

There are ten connectors on the SpaceFibre camera: four SpaceFibre connectors (2-lane nominal and 2-lane redundant), two SMA trigger input connectors, two SpaceWire connectors (nominal and redundant) and +5V DC power connectors (nominal plus JTAG and redundant plus configuration).

The image sensor is configured and controlled by an FPGA. The image sensor sends image data to the FPGA via 16 LVDS differential pairs running at up to 480 Mbits/s per pair. The FPGA includes four SpaceFibre lanes which can operate as two 2-lane links or one 4-lane link. When operating with two 2-lane links, one is active and the other is redundant. The FPGA transfers the image data out of the camera over the active SpaceFibre link. There are also two SpaceWire interfaces (nominal and redundant) which can be used for transferring data instead of using the SpaceFibre interfaces.

Camera configuration, control and housekeeping requests are received over virtual channel 0 of the active SpaceFibre link or over the active SpaceWire link when in SpaceWire interface mode. The FPGA interprets these commands and transfers information to and from the image sensor accordingly, using the control interface of the image sensor.

Attached to the image sensor is a bank of EDAC protected DDR memory which can be used to store images when the FPGA is being used as an image processor.

Power is provided to the SpaceFibre camera via a pair (nominal and redundant) of 15-pin micro-D connectors. The input power is DC-DC converted to the various power supplies required by the FPGA and image sensor. Power on reset circuitry is also provided to reset the FPGA and image sensor during power-up.

The JTAG interface for programming and debugging the FPGA is accessible using the spare pins of the nominal power connector. Six system configuration signals are similarly set using the spare pins of the redundant power connector. These six pins may also be used for debug input/output. The two SMA connectors provide two trigger inputs which are buffered using Schmitt triggers and passed to the FPGA.

A crystal oscillator is provided for the FPGA for general operation along with a programmable oscillator for the SpaceFibre links. A flexi connector is connected to spare pins of the FPGA for test and debug use.

The SpaceFibre camera electronics is implemented on a single flexi-rigid PCB as illustrated in Figure 2. The blue areas represent the rigid part of the PCB and the green the flexible part.

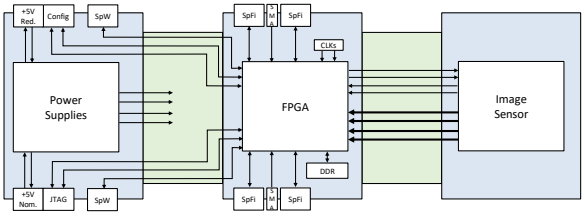

Figure 2: Flexi-Rigid PCB for SpaceFibre Camera

A physical model of the SpaceFibre Camera is shown in Figure 3 .

Figure 3: SpaceFibre Camera Physical Model

The SpaceFibre Camera is currently being manufactured. The final paper will provide results from testing the SpaceFibre camera in its various modes of operation.

4 SPACEFIBRE DATA PROCESSORS

In this section two SpaceFibre enabled data processing devices are described. The first is the SpaceVPX-RTG4 board which is a VITA78.1 SpaceVPX-Lite board, incorporating a Microsemi RTG4 FPGA. The second is the Ramon Chips RC64 many core DSP processor.

4.1 SpaceVPX-RTG4

The SpaceVPX-RTG4 board is a 3U board containing a radiation tolerant Microsemi RTG4 FPGA. A block diagram of this board is shown in Figure 4 along with a photograph in Figure 5.

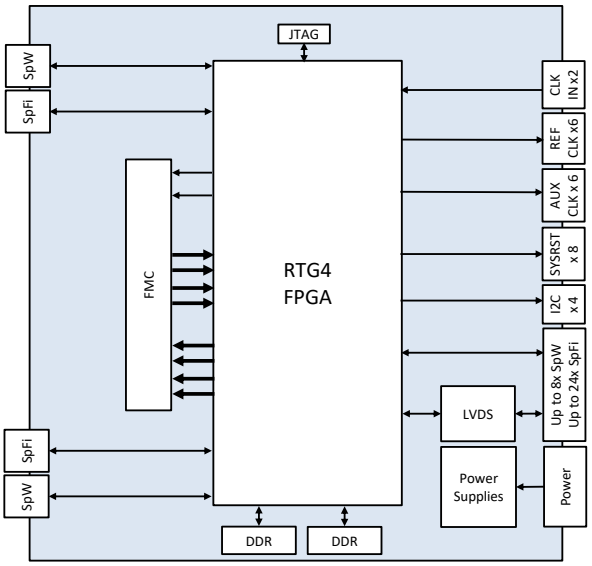

Figure 4: SpaceVPX-RTG4 Board Block Diagram

The RTG4 can be configured as either a SpaceVPX-Lite (VITA 78.1) system controller or a payload processor. It provides the following sets of signals to the SpaceVPX-Lite backplane:

- Power connections from the power switch module.
- Control plane comprising either six SpaceWire links or six, four-lane SpaceFibre links.
- I2C buses to the two power supplies and power switch, used for control and status monitoring of these boards.
- Eight system reset signals, which fan out radially to the six payload processors and to the power supply and switch board.
- Six reference clocks, which are sent radially to the payload processors.
- Six auxiliary clock (synchronisation or periodic pulse signals), which are also sent radially to the payload processors.
- A pair of clock inputs, which are used to derive the clock output signals when the board is acting as a system controller and which provide the nominal and redundant clock inputs when operating as a payload module.

Attached to the RTG4 are two banks of 32-bit wide DDR memory each with 8-bit EDAC parity. A pair of SpaceWire and a pair of SpaceFibre connectors are provided on the front panel of the SpaceVPX-RTG4

board. To provide additional input/output functions an FMC connector is provided on the board. Several FMC boards are being designed to operate with the SpaceVPX-RTG4 board, including a 2.4 Gsamples/s, dual ADC board.

Figure 5: SpaceVPX-RTG4 Board

4.2 RC64 Many Core DSP Processor

Ramon Chips have developed a many core DSP processing chip in radiation tolerant technology [9]. The RC64, is a novel rad-hard 64-core digital signal processing chip, with a performance of 75 MACS, 150 GOPS and 38 GFLOPS (single precision) and low power consumption, dissipating less than 10 Watts. The RC64 integrates sixty-four advanced DSP cores, a hardware scheduler, 4 MBytes of multi-port shared memory, a DDR2/DDR3 memory interface, and twelve 3.125 Gbps full-duplex, high-speed SpaceFibre serial interfaces.

The RC64 architecture is illustrated in Figure 6. A central scheduler assigns tasks to processors. Each processor executes its task from its cache storage, accessing the on-chip 4MByte shared memory only when needed. When task execution is done, the processor notifies the scheduler, which subsequently assigns a new task to that processor. Access to off-chip streaming channels, DDR2/DDR3 memory, and other interfaces happens only via programmable DMA channels. This approach simplifies software development and it is found to be very useful for DSP applications, which favour streaming over cache-based access to memory. Hardware events, asserted by communication interfaces, initiate software tasks through the scheduler. This enables high event rates to be handled by the many cores efficiently.

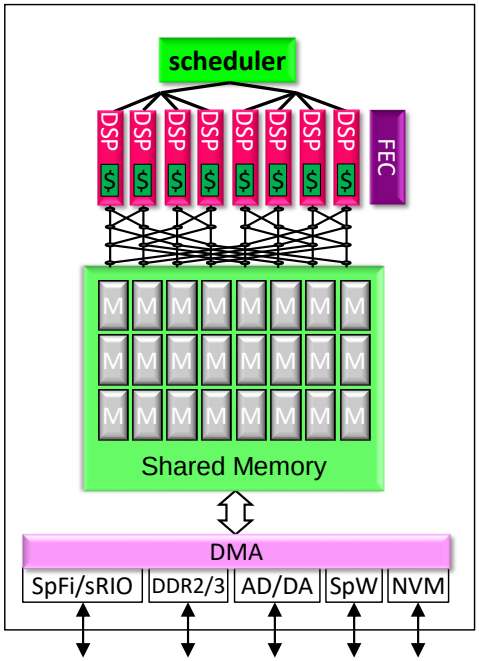

Figure 6: RC64 Many Core DSP Processor Block Diagram (only 8 DSP processors are shown)

The RC64 is implemented as a 300 MHz integrated circuit on a 65nm CMOS technology, assembled in a hermetically sealed ceramic CCGA624 package and qualified to the highest space standards. The 12 SpaceFibre interfaces on the RC64 were designed by STAR-Dundee.

5 CONCLUSIONS

SpaceFibre provides multi-gigabit/s communications. It incorporates a comprehensive quality of service capability providing integrated bandwidth reservation, priority and scheduling. Efficient, effective and rapid fault detection, isolation and recovery mechanisms are included in the SpaceFibre interface, enabling rapid detection and recovery from link level errors. SpaceFibre multi-laning allows the very high data rates to be achieved which are necessary for future SAR and multi-spectral imaging instruments.

The SpaceFibre Camera illustrates how easy it is to implement a high-performance image sensor in radiation tolerant technology, using SpaceFibre as the data and configuration, control and housekeeping interface into the instrument.

The SpaceVPX-RTG4 board illustrates how SpaceFibre can be incorporated into an FPGA based payload processing board, as both a high data-rate interface and a backplane interconnect.

The RC64 many core DSP processor illustrates how SpaceFibre can implement chip level interfaces

providing the high data-rate interfaces necessary to feed high performance signal and image processing devices.

The SpaceFibre standard will be published as an ECSS standard in mid-2018.

6 ACKNOWLEDGMENTS

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7 REFERENCES

[1] S. Parkes, A. Ferrer Florit and A. Gonzalez Villafranca, "SpaceFibre Standard", Draft K2, University of Dundee, December 2017.

[2] S. Parkes, C. McClements and M. Suess, "SpaceFibre", International SpaceWire Conference, St Petersburg, Russia, 2010, ISBN 978-0-9557196-2-2, pp 41-45.

[3] S. Parkes et al, "SpaceFibre: Multi-Gigabps Interconnect for Spacecraft On-board Data Handling", IEEE Aerospace Conference, Big Sky, Montana, 2015.

[4] A. Ferrer Florit, A. Gonzalez Villafranca and S. Parkes, "SpaceFibre Multi-Lane", International SpaceWire Conference, Yokohama, Japan, 2016, ISBN 978-0-9954530-0-5.

[5] ECSS Standard ECSS-E-ST-50-12C, "SpaceWire, Links, Nodes, Routers and Networks", Issue 1, European Cooperation for Space Data Standardization, July 2008, available from http://www.ecss.nl.

[6] S. Parkes, "SpaceWire Users Guide", ISBN: 978-0-9573408-0-0, STAR-Dundee, 2012, available from https://www.star-dundee.com/knowledge-base/spacewire-users-guide (last visited 11th Feb 2018).

[7] S. Parkes et al, "SpaceWire and SpaceFibre on the Microsemi RTG4 FPGA", IEEE Aerospace Conference, Big Sky, Montana, 2016

[8] S. Parkes, M. Dunstan et al, "A Wideband Spectrometer in the Microsemi RTG4 FPGA", DASIA, Oxford, May 2018.

[9] R. Ginosar, "RC64", IEEE Aerospace Conference, Big Sky, Montana, 2018.