SpaceFibre for FPGA: IPs and Radiation Test Results

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Abstract - SpaceFibre is a very high-performance, high-reliability and high-availability network for spaceflight applications. The latest advances in SpaceFibre IP cores for use in radiation-tolerant FPGAs are described. In addition, the results of the radiation campaign implementing SpaceFibre in the Microchip RTG4 FPGA are also presented. The goal of the campaign was to assess the impact of radiation in the performance of the in-built SerDes blocks and SpaceFibre. As expected, the SerDes blocks are sensitive to radiation. However, results also show that the use of SpaceFibre vastly mitigates the effects of radiation allowing to create reliable links even in these extreme conditions.

Keywords - SpaceFibre, SpaceWire, Radiation Testing, RTG4, PolarFire, KU060, SerDes, Transceiver, FPGA

Introduction

SpaceFibre (SpFi) is the next generation of SpaceWire (SpW) network technology for spacecraft on-board data-handling [1][2][3][4]. It runs over electrical or fibre-optic cables, operates at very high data rates, and provides in-built quality of service (QoS) and fault detection, isolation and recovery (FDIR) capabilities. Its high data rate per lane coupled with novel multi-lane technology enables SpFi to achieve very high performance: in excess of 20 Gbit/s with current space-qualified FPGAs and much higher in the near future. Its in-built error detection, isolation and recovery mechanisms enable rapid recovery from transient errors, without loss of data, providing high availability. Its multi-lane hot and cold redundancy features support high reliability. These capabilities are built into the hardware of each SpFi interface.

The SpaceFibre standard is an approved ECSS standard – ECSS-E-ST-50-11C [1].

SpaceFibre IP Cores

To support users of SpFi, STAR-Dundee has developed a comprehensive set of IP cores which are already being designed into their first spaceflight equipment and used in ASICs. The following IP cores are now available from STAR-Dundee targeted for radiation-tolerant FPGA and ASIC implementation:

- Single-lane interface
- Multi-lane interface
- Single-lane routing switch

A multi-lane routing switch IP core is under development with release planned for Q4 of 2020.

All these IP cores are fully configurable using VHDL generics and have been extensively validated. They are compliant to the ECSS standard.

a. Single-lane interface

The STAR-Dundee SpaceFibre Single-Lane IP core has the following features:

- Easy to use with a protocol agnostic interface. No prior knowledge of the SpFi standard is required. The SpW packet size, format and content are arbitrary.
- Validated in major FPGA families including radiation-tolerant devices, e.g. Microsemi RTAX, RTG4 and RT-PolarFire, and Xilinx Virtex-5QV, Spartan-6, Kintex-7 and UltraScale KU060.
- Supports lane rates up to 3.125 Gbit/s in RTG4 and Virtex-5QV, and 6.25 Gbit/s in Kintex UltraScale and RT-PolarFire.
- Highly configurable, giving flexibility through generics in the VHDL source.
- Simple data interfaces based on standard input and output FIFO interfaces (32-bit AXI4-Stream).
- Independent user-defined data read and write AXI clocks.
- Straightforward management interface, with optional statistics and debug signals.
- Automatically recovers from transient errors in less than 3 µs, without affecting the user data rate.

- Possibility to start one end of the link in a low-power mode waiting for the other end to become active.
- Optimised for low latency operation.
- Data and broadcast babbling node protection.
- Data integrity and reliable data delivery for BER better than 10^{-5}, and automatic lane disconnection when BER is worse than 10^{-5}.

b. Multi-lane interface

The STAR-Dundee SpaceFibre Multi-Lane IP core has been designed to be user friendly, with few configuration signals. In addition to the features of the Single-Lane IP Core, the Multi-Lane IP also provides:

- Configurable number of independent lanes with cold and hot redundancy. Any number of lanes supported (up to 16).
- Automatic graceful degradation in the event of a lane failure. When this happens the link BW is reduced, with higher priority Virtual Channels being less affected.
- Hot redundant lanes recover from lane failures in less than 3 µs without user intervention.
- Lanes can be configured as unidirectional to save power and mass in asymmetric data flows.
- Wide AXI4-Stream interface to support slow user clock.

c. Single-lane routing switch

The SpaceFibre routing switch connects several nodes with SpFi interfaces allowing them to talk to one another. The Router architecture is built around a non-blocking routing switch matrix and it is fully configurable: it allows any number of SpFi, SpW or FIFO-like ports. SpFi and FIFO ports can implement any number of virtual channels (VCs), each one comprising an input and an output VC buffer. A configuration port uses the RMAP protocol to configure the routing table, the links and their corresponding QoS. The STAR-Dundee SpaceFibre Routing Switch IP core is available as a single-lane IP core and will soon be available as a multi-lane IP core with a configurable number of lanes per port.

Implementation Footprint

The reduced implementation footprint of the SpFi IP core is one of its main features. The performance and capabilities of SpFi are excellent, but this is of no use if the implementation footprint requires a large part of a radiation-tolerant FPGA. The resource utilization for the Microchip and Xilinx FPGAs are provided in Table 1. Triple-mode redundancy (TMR) is not included in these figures.

The Microchip RTG4 is a radiation-hardened FPGA with 24 SerDes lanes (3.125 Gbit/s), which is being designed into many spaceflight units. The RT-PolarFire is a new radiation-tolerant FPGA from Microchip which is much larger than the RTG4 and includes higher speed transceivers (>6.25 Gbit/s). Figure 1 shows the SpFi Single-Lane IP implemented in a PolarFire FPGA, interfacing a STAR Fire EGSE unit.

Table 1: Resource utilization in various FPGAs

IP Core	Virtex-5QV XQR5VFX130	Spartan-6 XC6SLX150T	Kintex-7 XC7K325T	Kintex UltraScale KU060	RTG4 RT4G150	RT-PolarFire RTPF500T
Single-Lane Interface [1]	3.1% 3.3%	3.4% 1.4%	1.1% 0.7%	0.6% 0.4%	2.5% 1.8%	0.7% 0.6%
Multi-Lane Interface [2]	9.6% 11.7%	8.8% 5.1%	3.3% 2.2%	2.0% 1.4%	9.0% 6.8%	2.8% [4] 2.1%
Single-Lane Router [3]	40.5% 40.3%	38.4% 16.8%	14.5% 8.0%	8.6% 4.9%	31.7% 21.2%	9.2% [4] 7.4%

Top value: % LUTs. Bottom value: % of Registers. The specific IP core configurations detailed in the table are as follows:
[1] 2 virtual channels
[2] 4 lanes and 2 virtual channels
[3] Router with 8 SpFi ports (2 virtual channels each) and embedded RMAP configuration port
[4] Estimated values

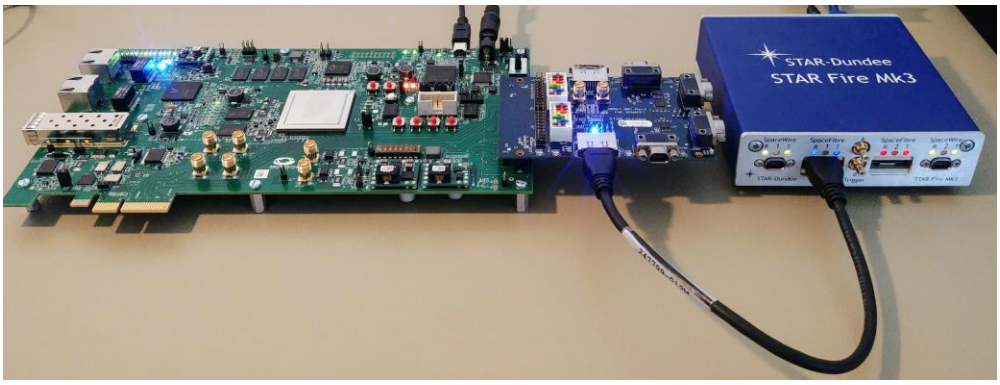

Figure 1: SpaceFibre running on a PolarFire FPGA and connected to the STAR Fire Mk3 EGSE

The Virtex-5QV and the UltraScale KU060 are Xilinx FPGAs which have been or are in the process of being qualified for space applications. In addition, various other Xilinx FPGAs have been or are being designed into spaceflight missions. The Virtex-5 and the Spartan-6 FPGAs have SerDes that are capable of 3.125 Gbit/s, while the Kintex-7 and UltraScale FPGAs have SerDes that can operate at 6.25 Gbit/s.

SpaceFibre Radiation Testing Running on the RTG4

The Microchip RTG4 FPGA features 6 SerDes blocks, each with 4 separate lanes. The SerDes analogue circuitry is radiation-hardened by design. However, the PMA configuration registers of the SerDes are not radiation-hardened (Section 4.1.2 of [5]) and a mechanism to minimise the effect of the radiation in these registers is required. For this reason, a radiation campaign was carried out at the TAMU Cyclotron facility in Texas, USA. Its purpose was to evaluate the performance of the SerDes under radiation, and to demonstrate the benefits of using SpaceFibre as a high-speed link in the RTG4 when subjected to radiation.

a. Test Set-Up

To achieve the objectives of the test campaign, different schemes were used for the different SerDes blocks available in the RTG4:

- SerDes #0 and #5 had all its lanes configured in PRBS mode and in PMA loopback. This mode is embedded in the SerDes IP and it generates a PRBS-31 pseudorandom sequence that is sent and received back, and subsequently checked for errors. The number of errors, together with the clock cycle where the first and last errors occurred, are available to the user in several registers [5]. A total of 8 lanes were operating in this mode to increase the volume of data gathered.
- SerDes #1 and #4 had 3 lanes each transmitting data over a SpFi multi-lane link. These lanes were all configured in PMA loopback. Internal data generators transmitted and received over the link. This data was checked upon reception. A total of 6 lanes were operating in this mode.
- SerDes #2 had a single lane transmitting data through a SpFi single-lane link. This lane was configured in PMA loopback. Internal data generators transmitted and received over the link. This data was checked upon reception.
- SerDes #3 had 2 lanes transmitting data through a SpFi multi-lane link. These lanes were connected to an external STAR Fire unit. Internal data generators generated data that was transmitted over the link and checked by the STAR Fire unit and vice versa.

An external reference clock source was supplied to SerDes #3 which was, in turn, distributed through a global output to the remaining SerDes blocks as a fabric clock input.

The breadboard used was the RTG4 development kit (RTG4-DEV-KIT) fitted with an unlidded PROTO silicon. The FMC-HPC1 port of the board was fitted with a SpW-SpFi FMC board from STAR-Dundee. Each board provides 2 SpFi interfaces (eSATA) and 4 SpW interfaces (9-pin micro-miniature D-type connector) that can then be used to interface the RTG4. An external SpW device (SpaceWire Brick Mk3) was connected to SpW Port 1 of the SpFi-SpW FMC board. This allowed access to the configuration and monitor registers. A STAR Fire Multi-Lane unit was connected to the two SpFi ports of the FMC board which were internally connected to SerDes #3. Figure 2 shows a block diagram of the set-up.

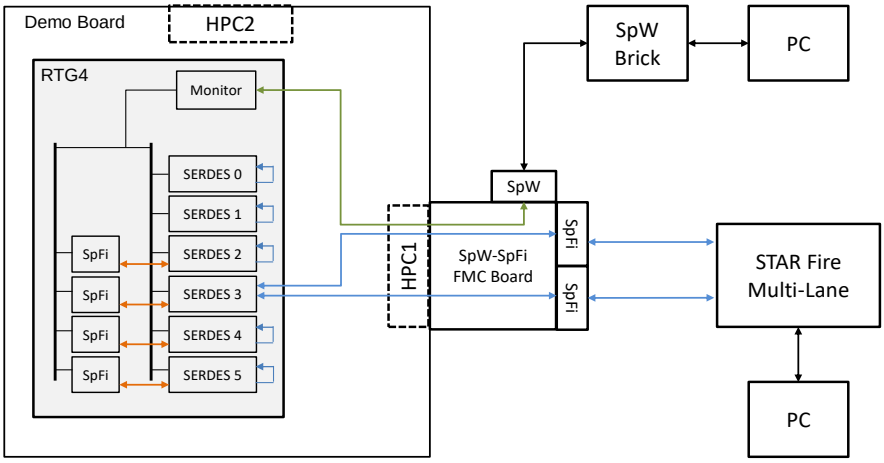

Figure 2: Block diagram of the test set-up

Note that due to limitations on the available hardware, the set-up of SerDes #3 was the most realistic one: it had an external reference clock source and it was connected to an external unit with a different reference clock. This was the only SerDes that was not connected in loopback.

Each SerDes had a *Monitor* module that configured the registers of the SerDes memory space over the APB bus. This module was also continuously monitoring the SerDes state and, whenever a failure was detected (i.e. error detected in the PRBS checker, or lane/link error in a SpFi link), a recovery procedure immediately followed. The values of the whole SerDes memory space were always recorded just before the recovery procedure allowing for a subsequent analysis of the event. On the other hand, the status and control registers related to the SpFi links were also being continuously monitored. This information was dumped periodically into log files that have been used to derive the results presented in this paper.

Figure 3 shows the test set-up inside the radiation chamber. On the left picture, the FPGA and the beam can be seen on the right side, and the rest of the hardware and controlling laptops in a trolley on the left. The right picture shows a close-up of the RTG4 FPGA with the beam source only a few mm apart.

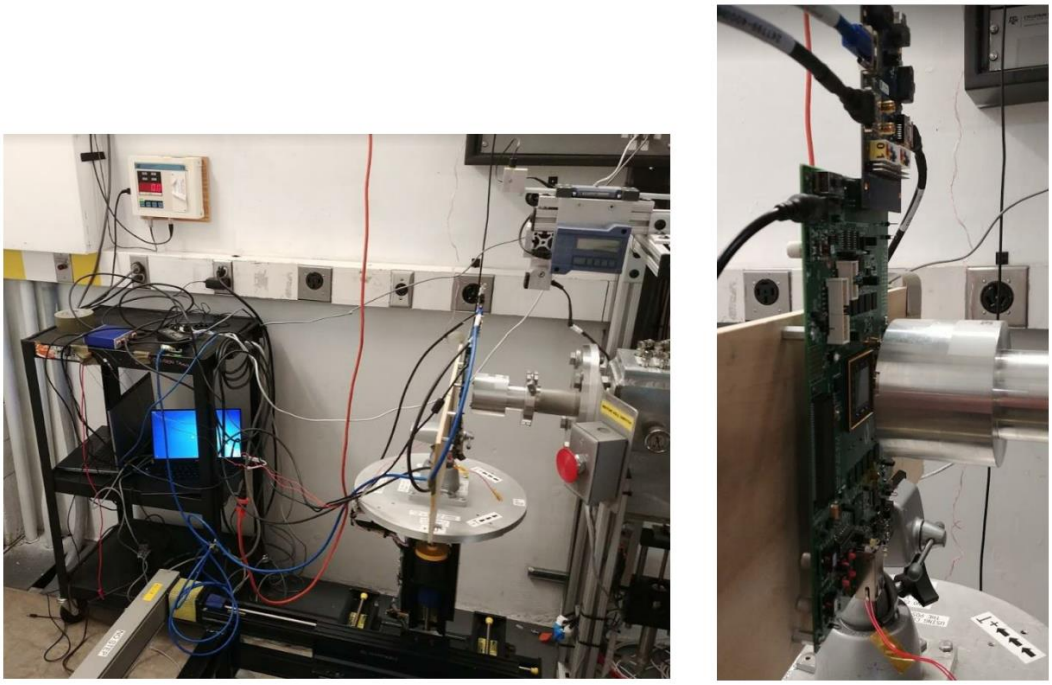

Figure 3: Test set-up inside the radiation chamber

b. SerDes Test Results

Two issues affecting the tests have been identified. Firstly, the operation of the internal 50 MHz clock oscillator (RCOSC) and its Lock output is affected by radiation. Unfortunately, part of the test control logic was using this clock: RCOSC Lock signal glitches caused all lanes of all SerDes to disconnect. Secondly, the Lock output of the Clock Conditioning Circuit (CCC) block is also affected by radiation. This was a more serious problem because the lock signal is used for the reset signal generation of the different clock domains. Therefore, glitches on this lock caused spurious resets of the SpFi IP Cores, the SerDes Error Recovery mechanism, and the data recollecting process.

These operational issues were mitigated by shielding from radiation the bottom corners (SE & SW) of the RTG4, which contain the RCOSC and CCCs used by the test control logic. Fortunately, the bottom corners did not contain any logic used by SerDes and SpFi links, so this shielding did not prevent radiation from reaching the rest of the design.

The PRBS test of SerDes #0 and #5 allowed to characterise the SerDes block behaviour under radiation. Figure 4 shows the cross section obtained for individual lanes. LET axis units are defined as [MeV·cm2/mg] for all the plots in this article.

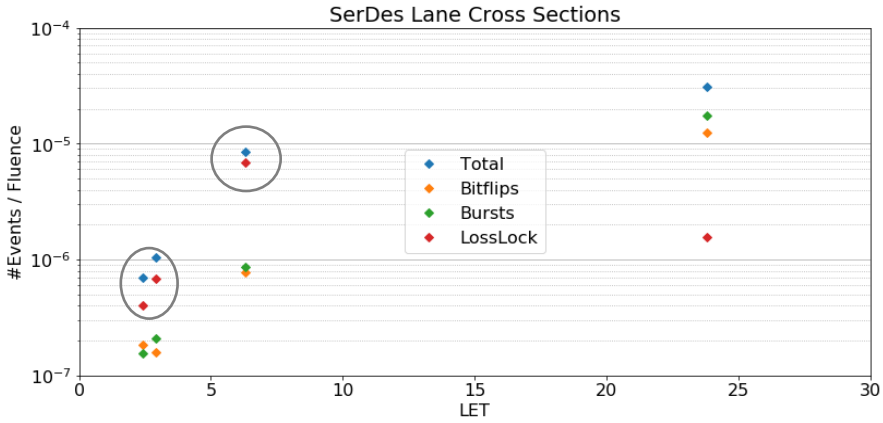

Figure 4: SerDes Lane cross-section for different types of error

The main results for the SerDes tests can be summarised as:

- Error bursts are much more frequent for higher LETs.
- The average length for a bit-flip event slightly increases for higher LETs, presenting a length between 2 and 4 PRBS words.
- The loss of lock values for the clock data recovery (CDR) mechanism (LossLock) were probably affected by the RCOSC Lock glitches (grey circles). These glitches caused resets in all SerDes. Note that at high LET the CDR loss of lock event is less likely, probably because the test at higher LETs had the CCCs and RCOSC shielded. Further radiation data is required to clarify this matter.

c. SpaceFibre Test Results

SpFi has an in-built error recovery mechanism that automatically recovers from transient (recovery in less than 3 µsec) and persistent errors on a SpFi link. Thanks to this fast recovery, transient errors occurring on the link do not affect user data throughput. Furthermore, several error detection mechanisms work concurrently to minimise the possibility of errors in the link being propagated to the user. This is essential in a radiation environment like space. Hence SpFi guarantees data integrity and reliable data delivery for a BER better than 10^{-5} and automatic lane disconnection when the BER is worse than 10^{-5}. Additionally, when using multiple lanes (i.e. multi-lane) SpFi supports bandwidth aggregation and automatic graceful lane degradation, spreading traffic over the remaining working lanes automatically in the event of a lane failure.

Table 2 defines the different statistics signals monitored for the SpFi links. Their cross section is shown in Figure 5. Again, grey circles indicate data affected by the RCOSC Lock glitches, which caused disconnections across all lanes.

Table 2: SpaceFibre protocol statistic signals

Parameter	Description
RX_ERROR	Increased for every clock cycle that SpFi is not receiving valid words (e.g. symbol alignment lost or 8B10B error)
RETRY	Increases for every error recovery operation
LANE_DISCONNECT	Increases when a lane disconnects (it will then reinitialise)
CRC8_ERR	Indicates a CRC error detected in a control word or broadcast frame
CRC16_ERR	Indicates a CRC error detected in a data frame containing virtual channel user data
EDAC_CORRECT	EDAC detected a bit-flip and was corrected
EDAC_FAIL	EDAC detected a multi-bit-flip that was NOT corrected
DATA_ERROR	Data checker outside the SpFi IP detected an error

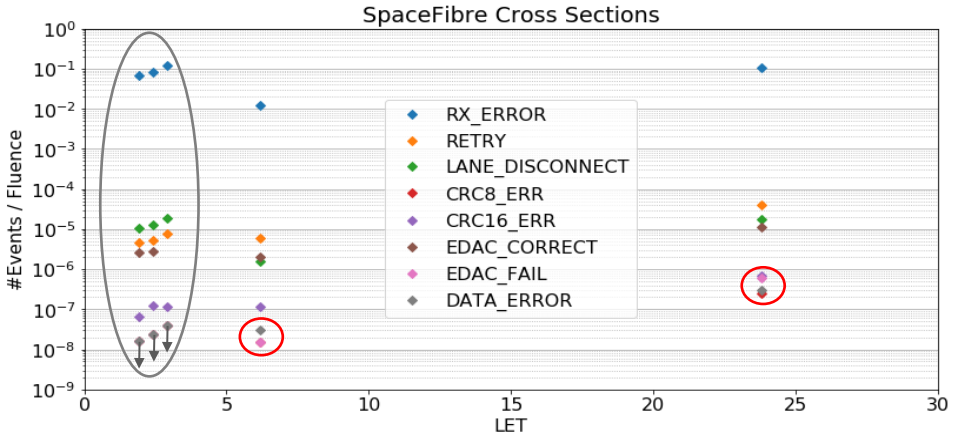

Figure 5: SpaceFibre cross-section for different types of error

Two main facts are worth noting. First, the number of protocol CRC errors is very low. Second, the SpFi data error cross section is close to that of the EDAC failure cross section (highlighted in red circles). These two facts imply that the few user data errors observed were not probably due to the SpFi protocol design (e.g. CRC event not detected) but to the radiation effects on the device fabric implementing the SpFi IP (e.g. EDAC failures). Therefore, it is possible to improve the SpFi resilience to radiation by ensuring data integrity in the event of an EDAC non-correctable error detected. This can be done simply by flushing the buffers and passing an Error End-of-Packet character to the user for EDAC errors.

On the other hand, the SpFi user data throughput was not significantly affected by radiation effects. In the tests the throughput, defined as the ratio between the total time and time receiving data without RXERRs, was better than 99.99% during irradiation even for high LET and high flux. Moreover, at 45 MeV·cm2/mg of equivalent LET the link connected to the STAR Fire unit was still showing full throughput, although unfortunately detailed statistical data could not be recorded.

Bit-flips and short burst errors are recovered by SpFi in less than 3 µs, although long burst errors require the lane to reinitialise (takes less than 30 µs). However, when using multi-lane link recovery in the event of one lane reinitialising continues to be lower than 4 µs, although with a temporarily reduced throughput until the failing lane recovers. Lane downtime, defined as the ratio between total time and the time in which the lane is reinitialising, was less than 0.005% for high LET and high flux.

The loss of lock events took between 100 and 200 µs to recover (TBC). The RCOSC Lock radiation effect was causing these events at low LETs. This event was unlikely at high LETs (i.e. cross section smaller than 2×10^{-6}), where the RCOSC component was shielded. In this case, a lane disconnection in one lane did not affect other lanes in the same or different SerDes blocks. This means that a multi-lane link recovers from a loss of lock event in less than 4 µs.

Finally, two anomalous events were recorded at high LET. In these two cases the affected lane required a few milliseconds to recover, but it did not affect other lanes. The estimated probability of the event is an order of magnitude lower than the probability of EDAC failure. This means that almost any other failure in the RTG4 will

occur before this anomaly. However, this needs further beam time to determine whether the anomalies are due to a real SerDes failure or other causes.

d. Simple Protocol vs SpaceFibre

Figure 6 presents the potential improvements from transferring data using the SerDes with a bespoke protocol without any correction mechanism to using the SpFi protocol. Again, grey circles indicate data affected by the RCOSC Lock glitches, which caused disconnections across all lanes. Note that when no protocol is being used, words in error (*SerDes Data Errors*) received due to *SerDes Failures* are assumed to be similar to the RX_ERROR SpFi protocol statistic. *SerDes Data Errors* is an average value but these error events will usually be concentrated in bursts due to the nature of failure types of the SerDes.

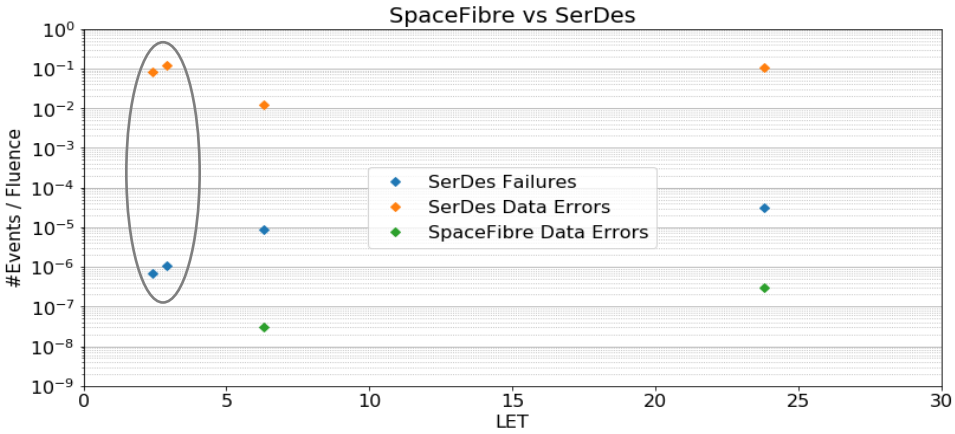

Figure 6: SpaceFibre versus SerDes operation

SpaceFibre provides full protection against SerDes radiation effects. At high LETs and fluence there can be a few data errors due to radiation effects on the IP Core logic, e.g. due to EDAC non-correctable errors. With the statistics of the IPs tested this would correspond to less than a data error every 10,000 years at GEO minimum and 100 mil Al. Furthermore, the number of errors could be further reduced with the application of additional mitigation techniques on the design of the IP Core, as outlined in the previous section.

Conclusions

SpaceFibre is now being integrated in many spacecraft equipment designs. It provides high-performance, high-reliability and high-availability, and has a small footprint in an FPGA. This makes it ideal for high-speed interconnect for connecting instruments, mass-memory, downlink transmitter, data compressor, payload processors and other equipment together on-board a spacecraft. The necessary IP cores and test equipment are available and being used to support such developments.

A campaign has been carried out to evaluate the performance of the RTG4 SerDes under radiation, and how the use of reliable protocols such as SpaceFibre can mitigate its effects. This campaign provided valuable information regarding the use of the CCC or local oscillator Lock signals. In the campaign set-up, a dedicated SerDes reconfiguration module recovered SerDes failures when the SpaceFibre protocol or the PRBS test indicated lane failure. The operation of this module has been validated: all SerDes recovered from the radiation failures without requiring a power cycle or a device reset. However, radiation effects on the SerDes produced temporary loss of lock, bit-flips and burst errors. This translates to a significant number of data errors when no protocol is used.

The campaign also showed the advantage of using SpaceFibre to protect against those radiation effects. SpaceFibre includes in-built error detection, isolation and recovery mechanisms that enable rapid recovery from transient errors, without loss of data. Transient errors are recovered in less than 3 µsec. Persistent errors are recovered in less than 30 µsec when using single-lane. In multi-lane, persistent and permanent errors are recovered in less than 4 µsec, with temporarily reduced throughput in case hot-redundancy is not used, supporting high reliability. At high LETs and fluence there can be a few data errors due to radiation effects on the IP Core logic, e.g. due to EDAC non-correctable errors. Following the test campaign, areas for improving the resiliency of the SpaceFibre IP have been identified and will be applied.

The results presented are preliminary. It is important to perform a second radiation test campaign with a revised design addressing all the issues identified in the first campaign. Further tests at higher LETs would allow to calculate LET Weibull curves and reduce error margins, and to obtain precise data about the lane disruption times.

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