STAR-Dundee

SpaceWire and SpaceFibre Expertise

SpaceWire Interface IP Core

SpaceWire is a data-handling network for use on-board spacecraft, which connects together instruments, mass-memory, processors, downlink telemetry, and other on-board sub-systems. SpaceWire has some specific characteristics that help it support data-handling applications in space.

STAR-Dundee offers essential SpaceWire interface and network components as VHDL IP blocks for use in FPGAs and ASICs. Our IP has proven to be robust and is widely used across the space industry, having been integrated into a number of flight FPGAs and flight ASICs.

Each of our SpaceWire IP cores has the following features:

- Delivered as synthesisable VHDL source code in obfuscated or clear code format
- Highly configurable, giving flexibility through generics in the VHDL source
- Easily targeted for major FPGAs including Microchip, Xilinx, Altera and NanoXplore. Support for radiation tolerant device features including the Microchip RTAX, ProASIC3E/L and RTG4.

Reference designs are available for Xilinx, Microchip and NanoXplore devices. Please contact STAR-Dundee for other target devices.

SpaceWire Interface IP

The STAR-Dundee SpaceWire Interface IP is a SpaceWire network interface block which is fully compliant with the ECSS-E-ST-50-12C Rev.1 SpaceWire standard.

Functions

The SpaceWire Interface IP is comprised of a SpaceWire protocol encoder and decoder, an initialisation state machine controller, receive and transmit data FIFOs with flow control management counters, and time-code interfaces for time distribution. Packet and Time-code interfaces are AXI4 Stream encoded. An overview of the IP functional blocks is shown in Figure 1.

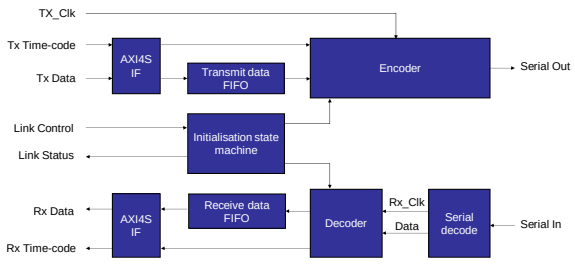

Figure 1. Interface IP Functional block overview

Interfaces

The IP core interfaces are shown in Figure 2 below.

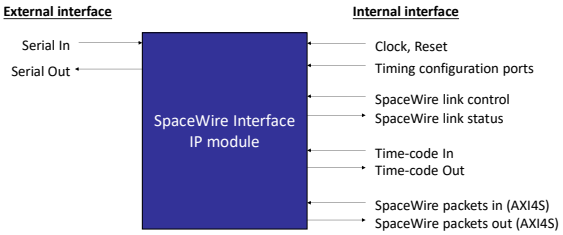

Figure 2. Internal and External interfaces

The internal interface to the application is comprised of AXI4 Stream parallel data and time-code interfaces. The parallel interface can easily be connected to RMAP, DMA and Router cores.

Features

The IP provides a highly flexible interface to SpaceWire with the following features:

- User AXI4 Stream packet interface with configurable data width
- Optional serial encoder bit clock
- Encoder Double Data Rate (DDR) option compatible with technology specific FPGA buffers
- FIFO storage instantiation in Fabric TMR protected flip-flops, HDL inferred RAM blocks, EDAC protected RTG4 uSRAM using RTG4 RAM64x18 primitives with ECC enabled or EDAC protected SRAM using a Microchip CoreEDAC core.
- Configurable FIFO size.

Device Utilisation

The approximate utilisation figures for a typical SpaceWire Interface IP implementation with 32-byte transmit and receive FIFOs is given in the table below. Xilinx FPGA results are obtained using XST or Vivado Synthesis. MicroChip results are obtained using Synplify synthesis.

Technology	LUT	FF	RAM
Xilinx Virtex 4QV (pre TMR tool)	802	544	2
Xilinx Virtex 5QV	597	537	2
Xilinx Zynq, 7-Series, Ultrascale, Ultrascale+	421	537	2
MicroChip ProASIC3 (E/L) – pre TMR	2075 Tiles		2
MicroChip RTAX	1055	565	2
MicroChip RTG4, IGLOO2, SmartFUSION2	732	536	2
MicroChip PolarFire	-	-	-
NanoXplore (NXMap 2.9.5)	536	457	2

Licensing

STAR-Dundee SpaceWire IP is available under license, provided as complete VHDL source code.

For more information on the IP cores, license, or if you have specific or custom requirements, please contact us.

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