STAR-Dundee

Supporting SpaceWire Applications

SpaceWire Physical Layer Tester

The SpaceWire Physical Layer Tester (SPLT) is a tool for testing the Physical and Signal Levels of the SpaceWire standard. It can determine the tolerance of a SpaceWire device to degraded LVDS signals by altering the SpaceWire LVDS output signals and exposing the input signals for measurement on an oscilloscope. Configurable parameters allow the amount of skew, jitter, swing and common mode voltage of the LVDS signals to be adjusted, either independently or collectively.

With interfaces to a host PC, a high bandwidth oscilloscope and a logic analyser, the SPLT can be connected in a variety of configurations to comprehensively test and explore the margins of the physical layer of a SpaceWire unit under test (UUT).

Key Features

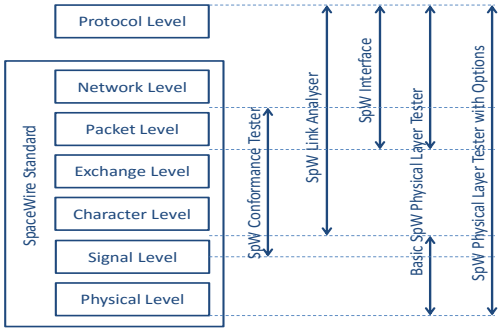
- Configurable Physical Layer characteristics:
  - Skew
  - Jitter
  - Swing
  - Common-mode voltage
- Test in different configurations:
  - In-Line analysis
  - Loop-Back testing
  - SpaceWire Router/Interface

NO SINGLE POINT OF FAILURE

The design of the SPLT electronics ensures that there is no single point of failure that could result in damage to SpaceWire equipment that it is connected to.

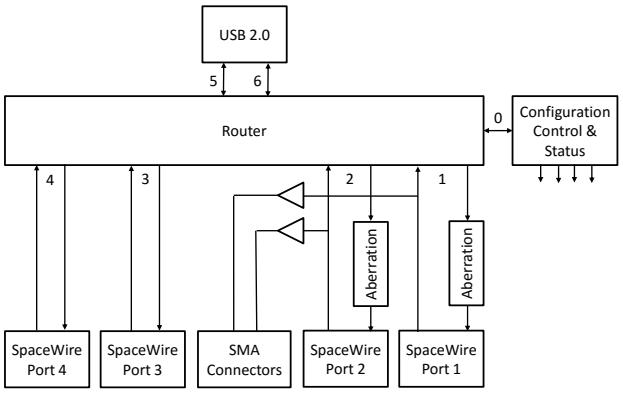
FMECA report available on request.

The Levels of the SpaceWire standard covered by the options are:



Overview

A block diagram of the SPLT is shown below:



The SPLT has two normal SpaceWire interfaces (ports 3 & 4) and two SpaceWire interfaces where the LVDS transmit signals can be altered to support physical layer margin testing (ports 1 & 2). Special aberration circuitry is able to adjust the in-pair and data-strobe skew, apply signal jitter, change the signal amplitude and adjust the common-mode voltage. Aberrations are made under control of software running on a host computer via the USB 2.0 port and the configuration, control and status circuitry.

The LVDS receive signals on ports 3 and 4 are buffered and passed to a set of SMA connectors for connecting to an oscilloscope. This permits eye pattern measurements on the receive signals to be made using a suitable oscilloscope.

Operating Modes

The SPLT has three basic operating modes.

In-Line Margin Analysis

The SPLT is connected between two SpaceWire UUTs for in-line analysis mode. The two UUTs communicate as normal, sending and receiving data to each other. The SPLT buffers incoming signals on one SpaceWire port and then drives them out through the analogue LVDS drivers on the other SpaceWire port. The SPLT can then manipulate the SpaceWire signals in one or both directions to explore the receive margins of either, or both, UUT devices.

Loop-Back Margin Analysis

The SPLT is connected to a single UUT to perform loop-back margin analysis. The SPLT receives data from the UUT and loops the data back through the same SpaceWire port. The LVDS transmitters on the SPLT can manipulate the data to test the receive margins of the UUT.

Interface and Routing Mode

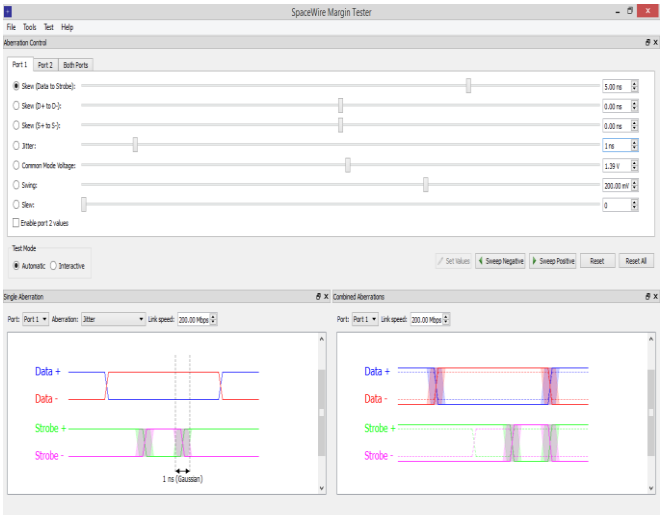
The SPLT incorporates a SpaceWire router so that packets can be routed between the four SpaceWire ports and between those ports and the USB ports. This makes switching of SpaceWire traffic through the pre-configured Physical Layer Test Ports very easy. The SPLT also supports the interface mode common to other STAR-System compatible devices.

Software

The SpaceWire Physical Layer Tester hardware is supported by specialised GUI software for margin testing and calibrating of the SPLT. These GUIs allow the user to easily control the type and amount of signal degradation, and quickly build sophisticated test scenarios to explore the tolerances of the device under test, or emulate the environment the device will be integrated into. Built on the foundations of STAR-System, the common suite of GUI applications for device configuration and packet handling are also provided.

Margin Tester

The Margin Tester GUI allows the user to control all the configurable Physical Level characteristics for manipulating the signals on either, or both SpaceWire ports. The signals can be controlled either interactively by the user using slider controls or setting specific values, or adjusted automatically until failure is detected. An aberration diagram below the sliders illustrates the effect of the aberrations on the signal. The user can adjust the aberrations until a UUT disconnects. The results can be recorded. Specific aberration values may be set and stored for use in "production" testing. These aberrations values set the required margin of operation that the UUT is required to have.



Calibrator

The Calibrator GUI allows the user to calibrate the SPLT hardware to ensure that the desired levels of aberration are applied. Calibration accounts for physical characteristics such as different cable lengths, temperatures, etc. This configuration then serves as the baseline reference for the Physical Layer Test ports from which the Margin Tester can alter the signals for Margin Analysis.

Supported Operating Systems

- Windows (32- and 64-bit Windows 8, 7, Vista, XP).
- Please enquire for Linux support.

Options

See www.star-dundee.com for details and availability of options.

Specifications

- **Physical Layer Test Ports:** Two special LVDS interface SpaceWire ports that facilitate the manipulation of the Physical Layer characteristics.
- **Skew:** 0 ns to +/- 8 ns in steps of approximately 0.01 ns.
- **Jitter:** 0 ns to +/- 8 ns in steps of approximately 0.01 ns
  - Sweep from 0 ns to maximum jitter value (Sawtooth).
  - Sweep from 0 ns to maximum jitter value and back again (Triangular).
  - Random, white noise jitter in range 0 ns to maximum jitter value (White).
  - Random, Gaussian jitter in range 0 ns to maximum jitter value (Gaussian).
- **Swing:** 0 V to 320 mV in steps of approximately 0.01 V.
- **Common-mode voltage:** 20 mV to 2.9 V in steps of approximately 0.01 V.
- **In built calibration:** The SPLT includes calibration software to simplify user calibration of the unit prior to testing.
- **Buffering of signals received at Physical Layer Test Ports:** The LVDS + and LVDS – signals from the data and strobe signals of each physical layer test port are buffered onto SMA connectors for direct connection to an oscilloscope. These buffered signals provide close representation of the signals at the receiver inputs.
- **SpaceWire Ports:** In addition to the physical layer test ports two normal SpaceWire ports are provided on the SPLT.
- **External triggers:** Four triggers are provided on the back panel of the SPLT to support the Link Analyser option.
- **Logic analyser interface:** A 38 pin MICTOR logic analyser connector is provided on the rear panel of the SPLT. The SpaceWire traffic in each direction of the link is decoded into a set of characters which are provided on the logic analyser connector, simplifying debugging. This is only used with the Link Analyser option.
- **USB 2.0 interface:** A USB 2.0 interface provides a high speed connection to a host PC or laptop to configure and control the SPLT, and provide the monitor and analysis displays.
- **SpaceWire Ports:**
  - Compliant to ECSS-E50-12A and ECSS-E-ST-50-12C
  - Number of SpaceWire Ports: 4
  - Speed: 2Mbits/s up to 200 Mbits/s
  - Connectors: 9-pin micro-miniature D-type
- **Exposed Oscilloscope Physical Layer Test Ports inputs:**
  - SpaceWire Data and Strobe LVDS + and LVDS - signals received on ports 1 and 2 are buffered onto 50Ω SMA connectors.
- **Trigger input and output ports:**
  - SMB connectors: +3.3V output signal, 5V input tolerant.
- **LEDs:**
  - Normal SpaceWire Ports: SpaceWire traffic indicators.
  - Physical Layer Test Ports: aberration mode and SpaceWire traffic indicators.
- **Size:** 220 x 115 x 30 mm (approx.).
- **Power:** +5V DC, 6A power brick supplied.
- **USB Port:** USB 2.0 (480 Mbits/s).
- **EMC:** CE/FCC certified.

FMECA report available on request

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