

# A Complete Set of SpaceFibre IP Cores in the New Generation of FPGAs for Space

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**Abstract**—SpaceFibre (ECSS-E-ST-50-11C) is a very high-performance, high-reliability and high-availability network technology specifically designed to meet the needs of space applications. It provides point-to-point and networked interconnections at Gigabit rates with Quality of Service (QoS) and Fault Detection, Isolation and Recovery (FDIR). SpaceFibre has been in use in at least two operational missions since 2021, with more missions in both Europe and the USA currently designing or planning to use SpaceFibre.

STAR-Dundee has developed a complete family of SpaceFibre IP cores fully compliant with the SpaceFibre standard. This family is composed of four different IPs: Single-Lane Interface, Multi-Lane Interface, Single-Lane Routing Switch and Multi-Lane Routing Switch.

A new generation of radiation-tolerant FPGAs is emerging to cope with the ever-growing processing power required by newer missions. Microchip has released the PolarFire RTPF500, Xilinx the Versal XQRVC1902, and NanoXplore the BRAVE NG-Ultra. SpaceFibre operation requires serial transceivers, which are already inbuilt in modern FPGAs. The IPs have been adapted to take advantage of the specific transceivers and memory blocks offered by these new FPGAs.

In this work we analyse in detail the performance of STAR-Dundee SpaceFibre IP cores on this new generation of FPGAs considering several performance metrics such as maximum lane speed, resource usage, etc. We also compare the performance of the IPs with current state-of-the-art space-grade FPGAs, Microchip's RTG4 and Xilinx's Kintex UltraScale XQRKU060. This analysis can also be used as a representative benchmark to compare the performances of the different FPGAs available for space applications.

**Keywords**—SpaceFibre, Interface, Routing Switch, IP Cores, PolarFire, RTPF500T, Versal, XQRVC1902, BRAVE, NG-Ultra, RTG4, UltraScale, XQRKU060

## I. INTRODUCTION

SpaceFibre (SpFi) [1] is a communication technology for use onboard spacecraft which was released as an ECSS standard in 2019 (ECSS-E-ST-50-11C). It provides point-to-point and networked interconnections at Gigabit rates while offering QoS and FDIR capabilities. SpFi interoperates seamlessly with a SpaceWire (SpW) [2] network over virtual channels (VCs) as it uses the same data packet definition. Furthermore, SpFi provides broadcast capabilities and can operate over either copper or fibre optic cables. To enhance throughput and robustness, SpFi links can also operate as multi-lane, thus allowing data of a single logical link to be spread over several individual physical lanes. This multi-lane

operation provides higher data rates through lane aggregation, supporting any number of lanes (up to 16) and unidirectional operation. This effectively multiplies the throughput of the interface by combining several lanes into a link. Furthermore, when a lane fails the multi-lane mechanism supports hot and warm redundancy and graceful degradation by automatically spreading traffic over the remaining working lanes.

The Network layer in SpFi is responsible for transferring data packets over a link or network. The routing concepts are the same as in SpW including both path and logical addressing. The Network layer includes the definition of Virtual Networks (VN). These VNs are built from the interconnection between VCs of different ports. VNs enable the creation of flexible SpFi routing switches (routers for short) comprising SpFi interfaces and a fully configurable, non-blocking, high performance routing switch.

STAR-Dundee has developed a range of SpFi IP cores compliant with the standard. The range is composed of four different IPs: Single-Lane Interface (SL Intf), Multi-Lane Interface (ML Intf), Single-Lane Router (SL Router) and Multi-Lane Router (ML Router). These IPs have been optimised for speed considering the timing constraints of the slower FPGAs for space.

STAR-Dundee SpFi IPs are TRL-9, currently flying in, and being designed into, several operational space missions. SpFi has also been tested in orbit in two demonstrator missions: NORBY and OPS-SAT [3].

## II. THE NEW GENERATION OF FPGAS FOR SPACE

There are two main devices that belong to the previous generation of space-qualified FPGAs. They both offer inbuilt high-speed transceivers that allow for the different SpFi IPs to be implemented. On the one hand, there is the Microchip RTG4. It uses non-volatile configuration memory and is manufactured in a low power 65 nm process [4], which is radiation-hardened by design. Thus, the big advantage of using the RTG4 is that Triple Module redundancy (TMR) has been integrated in its fabric transparently to the user. On the other hand, there is the Xilinx XQRKU060 [5]. It uses SRAM-based (volatile) configuration memory and is manufactured on a faster and more compact 20 nm process. This FPGA offers roughly four times the resources of the RTG4 but does not offer the same degree of hardening against radiation.

A new generation of FPGAs specifically targeting space applications has recently been or is in the process of being released. This new generation aims at higher performance applications, which makes them ideal targets for using very high-speed communications protocols such as SpFi.

### A. Microchip PolarFire

The radiation-tolerant PolarFire (PF) RTPF500T FPGA is directly derived from its commercial counterpart, a non-volatile FPGA built on a 28 nm process [6]. PF uses low-power SONOS configuration switches that have been demonstrated to be robust at 100 krad of total dose and having an absence of configuration upsets under heavy-ion single event tests. Like the RTG4, PF provides 24 transceivers but with a higher maximum speed (10 Gbit/s). Unlike radiation-hardened devices, depending on the application the Single Event Upset (SEU) rate of the PF registers may not be good enough. In this case, the use of some form of TMR is advised.

### B. Xilinx Versal

The Xilinx Versal XQRVC1902 [7] is the radiation-tolerant version of the commercial SRAM-based XCV1902 FPGA. It is manufactured in a 7nm FinFET technology and provides a platform aiming at high performance applications, offering 44 GTY transceivers (25 Gbit/s). Using TMR in Versal is also advised depending on the application and its requirement for register SEU sensibility, as the FPGA is not radiation-hardened.

### C. NanoXplore BRAVE

The NanoXplore BRAVE FPGA family is a European addition to the available options of space-qualified devices. There are several members of the BRAVE family, with the NG-Large [8] (65nm FD-SOI SRAM) and NG-Ultra [9] (28 nm FD-SOI SRAM) both including inbuilt SerDes blocks. These FPGAs are radiation hardened by design, which removes the need for TMR.

## III. SPACEFIBRE IP CORES GENERAL FEATURES

The STAR-Dundee SpFi IP core family has been extensively tested in the different space FPGA families. These IPs are provided with a protocol agnostic data interface, so that no prior knowledge of the SpFi standard is required. Simple data interfaces based on standard 32-bit input and output FIFO interfaces are used. Specifically, they follow the AXI4-Stream (AXI4-S) protocol [10], which is a popular industry standard, with independent user-defined read and write clocks.

The IPs can be configured using generics. Different properties can be configured, e.g. transceiver interface, target technology for direct memory instantiation (for EDAC use), number and size of VCs, etc. Different high-speed transceiver interface options provide the set of signals to be directly connected to the selected transceiver. A wrapper is supplied for each of the different transceiver interfaces for user convenience.

The QoS is independently and dynamically configurable for each VC. The FDIR mechanisms automatically recover from transient, persistent and permanent (when ML is used) errors on the SpFi link. A transient error takes less than 3  $\mu$ sec to recover. It does not affect the user data rate thanks to the embedded buffering inside the IPs. Other protections against errors include data and broadcast babbling node protection. A lane is automatically disconnected when the BER is worse than  $10^{-5}$  to prevent a potential protocol breakdown.

A management interface allows real time configuration of the IP control and status parameters, also including optional statistics and debug signals. Power management options have been considered. For example, it is possible of start one end of

the link in a low-power mode waiting for the other end to become active.

Two radiation testing campaigns have been carried out in collaboration with Microchip for the SpFi SL and ML Interfaces in the RTG4 [11, 12]. The information gathered during the test campaigns has allowed for assessing and further refining the robustness of the IPs under radiation and their associated RTG4 reference designs.

The IP Cores are also ready for ASIC implementation. For example, the SL Intf was used in the RC64 many-core DSP ASIC (12 SpFi interfaces) developed by Ramon.Space [13]. Other ASICs are currently under development also implementing the ML Intf and the Router IPs.

Full TMR has been applied to the IPs in the PF to assess its impact in performance. As expected, the resulting synthesis takes  $\sim 2.8$  times the number of initial registers (synchronisers are not triplicated) whereas the number of LUTs is increased by a factor of  $\sim 2$ . One possibility to reduce the impact of TMR on the IP is to apply partial TMR. The idea is to only protect the most critical parts of the IP, namely the control logic. This way, SEUs can induce sporadic data errors at the receiver, but the operation of the protocol itself is rugged against these events. This alternative is a compromise between full TMR and no TMR at all, and can be appropriate for certain applications which can tolerate a certain rate of data errors. This partial TMR is an ongoing development for the IPs here presented.

Finally, STAR-Dundee has adapted its SpFi IP Cores to be compatible with the BRAVE family. There is an ongoing activity to validate the operation of the IPs inside the NG-Ultra FPGA. Using a NG-Large a successful SpFi link has already been established, allowing the correct transmission of data between a STAR-Fire Mk3 unit and the NG-Large development board (Fig. 1) but sporadic retry events were observed during the IP validation. Thanks to the FDIR capabilities of SpFi data errors were always automatically corrected. The cause for these retries was tracked down to the clock scheme adopted, as the reference clock used for the SerDes was outside the specifications.



Fig. 1. BRAVE SpFi Interoperability Test with a STAR-Fire Mk3 unit.

### A. Timing Performance

Timing provided by the synthesis tools is not accurate, as the final timing depends on the routing and placement of the IP inside the FPGA fabric. Testing these IPs in different

configurations on different development boards have confirmed that the maximum lane speeds can be achieved with the RTG4 (3.125 Gbit/s) even for congested designs. The other FPGAs achieve lane rates beyond 6.25 Gbit/s with plenty of margin, thus allowing to operate at these high speeds even when using TMR on the design. BRAVE maximum speed is still an ongoing work since the tools are continuously improving.

#### IV. SPACEFIBRE SINGLE-LANE INTERFACE IP CORE

The resources required by the SL Intf IP for a different number of VCs are detailed in Table I. As the table shows, the IP offers a compact design only requiring a small percentage of area even when multiple VCs are used.

All the tables in this work include the transmit and receive FIFOs.

TABLE I. SPFI SINGLE-LANE INTERFACE RESOURCE USAGE

	RTG4			XQRKU060 *		
	LUT	DFP	LSRAM	LUT	DFP	RAMB36
<b>1 VC</b>	3040 2.0%	2219 1.5%	4 1.9%	1761 0.5%	2220 0.3%	4 0.4%
<b>2 VCs</b>	3657 2.4%	2801 1.8%	6 2.9%	2127 0.6%	2870 0.4%	6 0.6%
<b>4 VCs</b>	4878 3.2%	3940 2.6%	10 4.8%	2889 0.9%	4120 0.6%	10 0.9%
<b>8 VCs</b>	7108 4.7%	6180 4.1%	18 8.6%	4427 1.3%	6618 1.0%	18 1.7%

	RTPF500T *			XQRVC1902 *		
	LUT	DFP	LSRAM	LUT	DFP	RAMB36
<b>1 VC</b>	2765 0.6%	2126 0.4%	8 0.5%	1609 0.2%	2220 0.1%	4 0.4%
<b>2 VCs</b>	3337 0.7%	2706 0.6%	12 0.8%	1941 0.2%	2871 0.2%	6 0.6%
<b>4 VCs</b>	4435 0.9%	3840 0.8%	20 1.3%	2713 0.3%	4140 0.2%	10 1.0%
<b>8 VCs</b>	6511 1.4%	6073 1.3%	36 2.4%	4264 0.5%	6619 0.4%	18 1.9%

	NG-Ultra		
	LUT	DFP	RAM
<b>1 VC</b>	2523 0.5%	2308 0.5%	8 1.2%
<b>2 VCs</b>	3035 0.6%	2913 0.6%	12 1.8%
<b>4 VCs</b>	4049 0.8%	4098 0.8%	20 3.0%
<b>8 VCs</b>	5900 1.1%	6427 1.3%	36 5.4%

\* TMR not included.

#### V. SPACEFIBRE MULTI-LANE INTERFACE IP CORE

##### A. Specific Features

Multi-lane is an optional capability of a SpFi link. The Multi-Lane layer coordinates the operation of multiple lanes acting as a single SpFi link, providing higher data throughput and redundancy. The number of lanes is fully configurable, with any number of lanes supported (up to 16). Each lane can independently be selected as uni/bidirectional and hot/warm redundant. In case of lane failure in a link without redundant lanes, the link is automatically reconfigured to continue with the remaining working lanes, hence producing an automatic graceful degradation of the link bandwidth. The QoS mechanism ensures that the most important data is sent first,

i.e. higher priority VCs or scheduled traffic are less affected. These capabilities are very useful for space applications where strict power constrains and a high level of reliability is required on the harsh space environment.

Fig. 2 shows the ML Interface IP being tested in a PF with 2 lanes coming out of a STAR-Dundee SpW/SpFi FMC daughterboard.



Fig. 2. SpFi ML on a PolarFire connected to a STAR-Ultra PCIe unit.

##### B. Area Resources

Table II provides the FPGA resource usage for a combination of different number of lanes (2, 4 and 8) and VCs (1 and 4). Individual lanes can operate up to 3.125 Gbps in the RTG4 and in excess of 6.25 Gbit/s in the rest of devices. This means aggregate rates with 8 lanes of up to 25 Gbit/s in the RTG4 and 50+ Gbit/s in the other devices.

TABLE II. SPFI MULTI-LANE INTERFACE RESOURCE USAGE

	RTG4			XQRKU060 *		
	LUT	DFP	LSRAM	LUT	DFP	RAMB36
<b>2 Ln 1 VC</b>	6831 4.5%	5499 3.6%	8 3.8%	3087 0.9%	4608 0.7%	8 0.7%
<b>2 Ln 4 VCs</b>	9112 6.0%	7759 5.1%	20 9.6%	4376 1.3%	6861 1.0%	20 1.9%
<b>4 Ln 1 VC</b>	13025 8.6%	9698 6.4%	16 7.7%	5612 1.7%	7687 1.2%	12 1.1%
<b>4 Ln 4 VCs</b>	15701 10.3%	12830 8.5%	40 19.1%	7102 2.1%	10807 1.6%	30 2.8%
<b>8 Ln 1 VC</b>	28591 18.8%	18111 11.9%	32 15.3%	11610 3.5%	13854 2.1%	20 1.9%
<b>8 Ln 4 VCs</b>	32074 21.1%	22987 15.1%	80 38.3%	13997 4.2%	18704 2.8%	50 4.6%

	RTPF500T *			XQRVC1902 *		
	LUT	DFP	LSRAM	LUT	DFP	RAMB36
<b>2 Ln 1 VC</b>	5478 1.1%	4255 0.9%	12 0.8%	2856 0.3%	4609 0.3%	8 0.8%
<b>2 Ln 4 VCs</b>	7782 1.6%	6509 1.4%	30 2.0%	4141 0.5%	6861 0.4%	20 2.1%
<b>4 Ln 1 VC</b>	10015 2.1%	7210 1.5%	20 1.3%	5141 0.6%	7686 0.4%	12 1.2%
<b>4 Ln 4 VCs</b>	12680 2.6%	10336 2.1%	50 3.3%	6717 0.7%	10804 0.6%	30 3.1%
<b>8 Ln 1 VC</b>	22798 4.7%	13129 2.7%	36 2.4%	11151 1.2%	13843 0.8%	20 2.1%
<b>8 Ln 4 VCs</b>	26198 5.4%	17999 3.7%	90 5.9%	13005 1.4%	18690 1.0%	50 5.2%

	NG-Ultra		
	LUT	DFP	RAM
2 Ln	5670	5719	16
1 VC	1.1%	1.1%	2.4%
2 Ln	7563	8069	40
4 VC	1.4%	1.6%	6.0%
4 Ln	10811	10086	32
1 VC	2.0%	2.0%	4.8%
4 Ln	13032	13343	80
4 VC	2.4%	2.6%	11.9%
8 Ln	23731	18835	64
1 VC	4.4%	3.7%	9.5%
8 Ln	26621	23906	160
4 VC	5.0%	4.7%	23.8%

\* TMR not included.

## VI. SPACEFIBRE SINGLE-LANE ROUTER IP CORE

The Router architecture is built around a non-blocking routing switch matrix with a configurable number of ports. Ports can be either SpFi, SpW or AXI4-S interfaces. Each port implements a configurable number of VCs. Each VC has an associated VN number. The switch matrix interconnects one or more VCs with the same VN number, with the limitation that each of these VCs must be in a different port. The output port is selected using path or logical addressing, indicated by the leading byte of each packet and the configuration of the internal routing table. Packets belonging to different VNs never interfere with one another and do not impact the throughput and latency within the routing switch matrix. On the other hand, when multiple packets in the same VN need to be transferred to the same output port, packet-by-packet arbitration is performed, exactly like in a SpW Router.

Fig. 3 shows a simplified Router. Note that SpW ports only have associated a single VC. The configuration port uses the RMAP protocol [14] to configure the routing table, VNs, Router ports, etc. Nevertheless, a dedicated AXI4-Lite interface can also be used to access the same configuration registers.

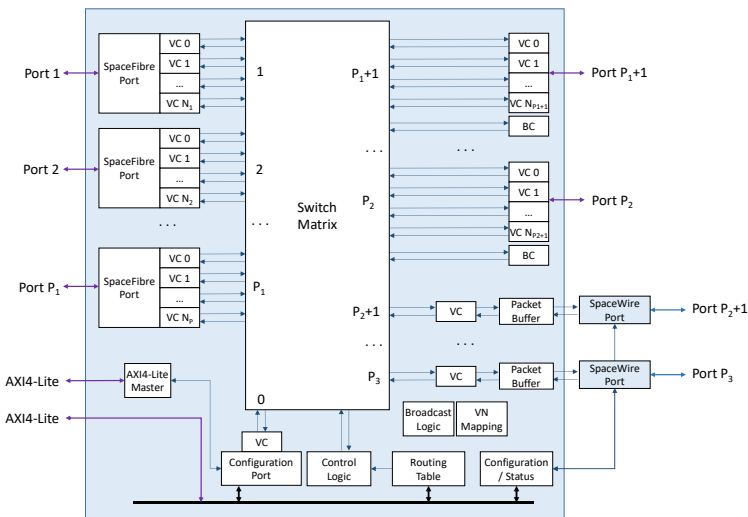


Fig. 3. SpaceFibre Router Block Diagram.

### A. Specific Features

The STAR-Dundee SpFi SL Router IP is a scalable, fully configurable non-blocking router. The IP is very flexible, allowing to select the number of VCs, ports and target technology, among other options, using generics. The SpFi lane rates are also configurable. The Router IP presents a

deterministic low latency switching. This Router implements path and logical addressing, VNs, time distribution and message broadcasting. VNs can be statically (fixed using VHDL constants) or dynamically configured, with up to 64 different VNs supported. There are up to 256 broadcast channels with higher priority for time-critical broadcast messages. The Router offers a simple and efficient integration with SpW networks using SpW packet buffers and automatic SpW to SpFi broadcast translation. An internal timer tracks time being distributed over the network.

An internal AXI4-Lite master allows accessing an external memory space using the extended address (0x1) capability of the RMAP protocol. Whenever the configuration port receives an RMAP command with extended address 0x1, the register access is carried out via this external AXI4-Lite interface. This can be useful when integrating the SpFi Router IP in a design with a companion instrument, for example. Another AXI4-Lite interface (slave) is available and allows doing the opposite access: accessing the internal memory space of the Router from an external device. This can be useful to configure the Router from a companion CPU.

Fig. 4 shows the SpFi SL Router IP testing on Versal with 4 different SpFi ports connected to a STAR-Ultra PCIe unit.

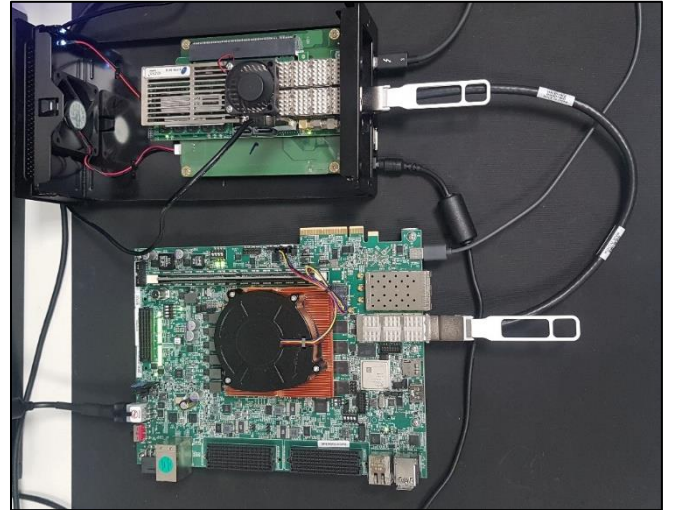


Fig. 4. SpFi Single-Lane Router on a Versal.

### B. Area Resources

Table III presents the resource usage for two different Router configurations which have been adopted as reference: a 4 SpFi port Router each with 2 VCs (4P 2 VC), and an 8 SpFi port Router each with 4 VCs (8P 4 VC). The table shows that even a “large” Router of 8 SpFi single-lane ports with 4 VCs (1L8P 4 VC) fits inside an RTG4. The SpFi SL Interface logic of the ports is included in the table figures, as well as the additional RMAP configuration port and all the configuration logic (see Fig. 3).

There are options to reduce the resource usage by tailoring the behaviour of the Router VNs. For some applications, provided that the network requirements are fixed, it is possible to limit the number of ports that can be accessed from a certain VN, thus helping to reduce the area of the design.

## VII. SPACEFIBRE MULTI-LANE ROUTER IP CORE

The STAR-Dundee SpFi ML Router IP is directly derived from the SL Router. It provides the same functionality but with a configurable number of lanes on the SpFi ML ports.

The main difference, apart from the ML interfaces, is that the internal data path width is increased accordingly—including the AXI4-S internal ports—so that the internal clock frequency of the Router does not scale up with the number of lanes.

The scenarios analysed for the ML Router are identical to the SL Router, with the difference that all SpFi ports have either 2 or 4 lanes (2L or 4L). Table III also includes the results for these multi-lane scenarios.

TABLE III. SpFi ROUTER RESOURCE USAGE

	RTG4			XQRKU060 *		
	LUT	DFP	LSRAM	LUT	DFP	RAMB36
<b>1L4P</b> <b>2 VCs</b>	26611 17.5%	25591 16.9%	36 17.2%	15473 4.7%	24946 3.8%	38 3.5%
<b>1L8P</b> <b>4 VCs</b>	84992 56.0%	74364 49.0%	120 57.4%	50871 15.3%	73691 11.1%	122 11.3%
<b>2L4P</b> <b>2 VCs</b>	45785 30.2%	42909 28.3%	63 30.1%	23391 7.1%	38333 5.8%	67 6.2%
<b>2L8P</b> <b>4 VCs</b>	132960 87.6%	112567 74.1%	203 97.1%	72101 21.7%	103514 15.6%	211 19.5%
<b>4L4P</b> <b>2 VCs</b>	77586 51.1%	67697 44.6%	113 54.1%	42066 12.7%	58412 8.8%	92 8.5%
<b>4L8P</b> <b>4 VCs</b>	N/A	N/A	N/A	117510 35.4%	150026 22.6%	292 27.0%

	RTPF500T *			XQRVC1902 *		
	LUT	DFP	LSRAM	LUT	DFP	RAMB36
<b>1L4P</b> <b>2 VCs</b>	25897 5.4%	25147 5.2%	72 4.7%	14163 1.6%	24908 1.4%	38 3.9%
<b>1L8P</b> <b>4 VCs</b>	83953 17.5%	73365 15.3%	240 15.8%	47311 5.3%	73679 4.1%	122 12.6%
<b>2L4P</b> <b>2 VCs</b>	40908 8.5%	37739 7.8%	99 6.5%	21308 2.4%	38387 2.1%	67 6.9%
<b>2L8P</b> <b>4 VCs</b>	125054 26.0%	102151 21.2%	323 21.3%	65201 7.2%	103632 5.8%	211 21.8%
<b>4L4P</b> <b>2 VCs</b>	66733 13.9%	58135 12.1%	149 9.8%	34048 3.8%	58433 3.2%	92 9.5%
<b>4L8P</b> <b>4 VCs</b>	193698 40.3%	149475 31.1%	485 31.9%	100234 11.1%	150040 8.3%	292 30.2%

	NG-Ultra		
	LUT	DFP	RAM
<b>1L4P</b> <b>2 VCs</b>	22087 4.1%	26615 5.3%	72 10.7%
<b>1L8P</b> <b>4 VCs</b>	70543 13.1%	77339 15.3%	240 35.7%
<b>2L4P</b> <b>2 VCs</b>	38002 7.1%	44625 8.8%	126 18.8%
<b>2L8P</b> <b>4 VCs</b>	110357 20.6%	117070 23.2%	406 60.4%
<b>4L4P</b> <b>2 VCs</b>	64396 12.0%	70405 13.9%	226 33.6%
<b>4L8P</b> <b>4 VCs</b>	N/A	N/A	N/A

SpFi Interface IP resources are included.

\* TMR not included.

The RTG4 does not allow for many SpFi ML ports as it has not enough resources for the design to fit. However, the rest of the FPGAs can implement large Routers using 4-lane SpFi ports for a total of 33 VCs (no TMR) while still having a considerable amount of free space for other applications if required.

This IP has been used to build the primary element of the Hi-SIDE project, the STAR-Tiger, a 10 SpFi port ML Router with 4- and 2-lane ports [15] developed using a Kintex UltraScale (Fig 5).

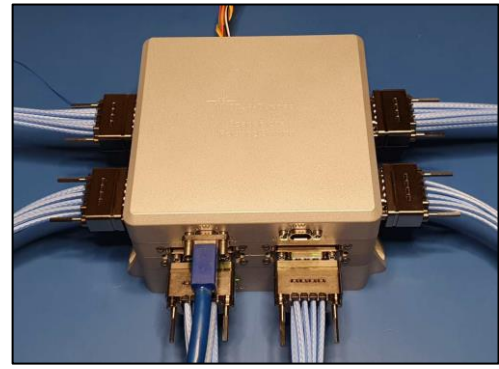


Fig. 5. STAR-Tiger SpaceFibre Multi-Lane Router.

## VIII. CONCLUSIONS

The STAR-Dundee SpaceFibre Single-Lane Interface, Multi-Lane Interface, Single-Lane Router and Multi-Lane Router IP Cores have been designed to be easy to implement in radiation-tolerant FPGAs. In this article we have detailed the performance and capabilities of the different IP Cores, and discussed the resources required depending on several parameters, namely the number of VCs, lanes and ports. All these IP Cores have been extensively verified in simulation and subsequently validated with different hardware prototypes.

A simple SpFi Single-Lane Interface (1 VC) can be integrated in radiation-hardened FPGAs by using only a 2% of an RTG4 and less than 0.5% in the other FPGAs analysed. This offers a simple way for implementing a high-speed and resilient communication channel in an FPGA. The multi-lane capability increases the data throughput of SpFi and the addition of multiple lanes provides hot and warm redundancy, or graceful degradation of the link bandwidth when no redundant lanes are available. Therefore, if more bandwidth or additional robustness is required out of a SpFi link, the Multi-Lane Interface IP is a convenient choice, keeping resource usage at a mere 4% for the RTG4 and 1% or less for the other devices. Finally, the SpFi Routers (SL and ML) can also be integrated in space-qualified FPGAs even when many ports are required.

These IPs provide the all the necessary building blocks for creating next generation of onboard networks. This has been demonstrated in the Hi-SIDE project, a European Union project involving several European aerospace organisations that have developed satellite data-chain technologies for future Earth observation and telecommunication systems [15]. The different elements of the data chain are interconnected via a SpFi network.

SpFi is at TRL 9 - already in operation in space, and it is also currently being implemented in FPGA and ASIC designs by different missions and products all over the world.

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