SpaceFibre Implementation, Test and Validation

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ABSTRACT

SpaceFibre is a very high-speed serial data-link be developed by the University of Dundee for European Space Agency (ESA) which is intended use in data-handling networks for high data-r payloads. SpaceFibre is able to operate over fibre-op and electrical cable and supports data rates of 2 Gb in the near future and up to 5 Gbit/s long-term. It ai to complement the capabilities of the widely u SpaceWire onboard networking standard: improv the data rate by a factor of 12.5, reducing the ca mass and providing galvanic isolation. Multi-lan improves the data-rate further to well over 20 Gbits/s

This paper provides an introduction to SpaceFibre a then describes the work being done by vari organisations to simulate, implement, test and valid SpaceFibre.

1 INTRODUCTION

SpaceFibre [1] [2] [3] [4] is a multi-gigabit/s serial network technology being designed specifically for spaceflight applications. SpaceFibre aims to support high data-rate payloads, for example synthetic aperture radar and hyper-spectral optical instruments. It provides robust, long distance communications for launcher applications and supports avionics applications with deterministic delivery capability.

SpaceFibre provides a quality of service mechanism able to support priority, bandwidth reservation and scheduling. It incorporates fault detection, isolation and recovery (FDIR) capability in the interface hardware. It is designed to be implemented efficiently, requiring only three times the number of logic gates of a SpaceWire [5] interface while providing many capabilities missing from SpaceWire.

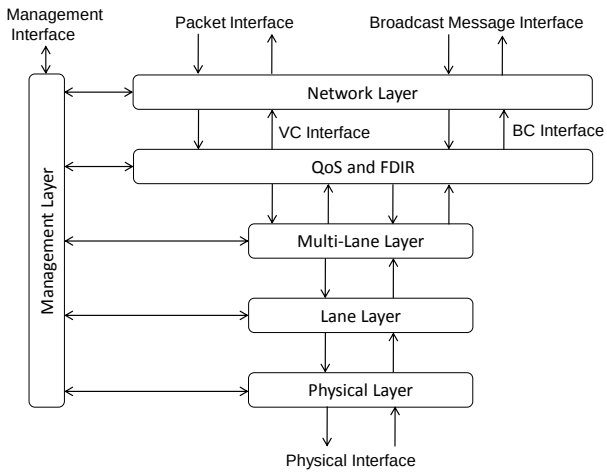

Fig. 1. SpaceFibre Protocol Stack

The network layer protocol is responsible for the transfer of application information over a SpaceFibre network. It provides two services: Packet Transfer Service and Broadcast Message Service. The Packet Transfer Service transfers SpaceFibre packets over the SpaceFibre network, using the same packet format and routing concepts as SpaceWire uses. SpaceFibre supports both path and logical addressing. The broadcast message service is responsible for broadcasting short messages (8 bytes) to all nodes on the network. These messages can carry time and synchronisation signals and be used to signal the occurrence of various events on the network.

The management layer is responsible for configuring, controlling and monitoring the status of all the layers in the SpaceFibre protocol stack. For example it can configure the QoS settings of the virtual channels in the QoS and FDIR layer.

The QoS and FDIR layer is responsible for providing quality of service and managing the flow of information over a SpaceFibre link. It frames the information to be sent over the link to support QoS and scrambles the packet data to reduce electromagnetic emissions. The QoS and FDIR layer also provides a retry capability, detecting any frames or control codes that go missing or arrive containing errors and resending them. With this inbuilt retry mechanism SpaceFibre is very resilient to transient errors.

The Multi-Lane layer is responsible for operating several SpaceFibre lanes in parallel to provide higher data throughput. In the event of a lane failing the Multi-Lane layer provides support for graceful degradation, automatically spreading the traffic over the remaining working links.

The Lane layer is responsible for lane initialisation and error detection. In the event of an error the lane is automatically re-initialised. The Lane layer encodes data into symbols for transmission using 8B/10B encoding and decodes these symbols in the receiver. 8B/10B codes are DC balanced supporting AC coupling of SpaceFibre interfaces.

The Physical layer is responsible for serialising the 8B/10B symbols and for sending them over the physical medium. In the receiver the Physical layer recovers the clock and data from the serial bit stream, determines the symbol boundaries and recovers the 8B/10B symbols. Both electrical cables and fibre-optic cables are supported by SpaceFibre.

3 SPACEFIBRE VALIDATION

The SpaceFibre standard has been written by the University of Dundee for ESA and has been widely reviewed by the international spacecraft engineering community. It has also been simulated and implemented in several forms. SpaceFibre is currently being integrated into several third party beta test applications to help refine the standard. The following sub-sections describe the various activities relating to the definition, implementation and validation of SpaceFibre.

3.1 Standard specification

The University of Dundee designed the lane layer of SpaceFibre with funding from ESA under the SpaceFibre contract, and the QoS and FDIR layer with funding from the European Commission (EC) SpaceWire-RT grant. The physical, multi-lane and management layers are currently being specified with ESA funding under the SpaceWire Demonstrator contract. At the moment of writing the current version of the SpaceFibre standard specification is draft F3, which is available from the SpaceWire Working Group website [1]. Work on the formal European Cooperation for Space Standardization (ECSS) standard for SpaceFibre is scheduled to start in the summer of 2014, once the technical specification is complete.

3.2 Simulation

As SpaceFibre was being designed by the University of Dundee, various alternative designs were simulated and traded-off with ad hoc software implementations. The aim of this simulation work was to rapidly explore alternative designs rather than provide formal validation of the standard specification.

During the SpaceWire-RT EC Framework 7 project, St. Petersburg University of Aerospace Instrumentation, performed extensive simulation of the SpaceFibre standard using SML to validate the available levels of the SpaceFibre specification and System-C to explore network level attributes of SpaceFibre. Feedback on issues and errors in the SpaceFibre specification was given for drafts C, D and E [6].

As part of the current ESA SpaceFibre Demonstrator activity Thales Alenia Space France (TAS-F) will be developing an OpNet simulation of the entire SpaceFibre protocol stack and validating its operation and the standard specification [7].

3.3 SpaceFibre IP core

In parallel with specifying the SpaceFibre standard the University of Dundee designed and tested a VHDL IP core for SpaceFibre. This was necessary to ensure that an implementation of SpaceFibre was efficient in terms of both performance and gate count. The SpaceFibre IP core was implemented in an FPGA to help test and validate the SpaceFibre specification. The IP core was used at all stages of the draft specification to validate and prove the concepts being explored. As a consequence, the VHDL IP core has gone through as many iterations as the SpaceFibre specification. At present the VHDL IP core implements all layers of the SpaceFibre specification with the exception of the Multi-Lane layer. This VHDL IP core is available from STAR-Dundee Ltd [8].

Within the EC SpaceWire-RT project one of the partners, ELVEES a Russian leading chip design company, explored the feasibility of implementing the SpaceFibre in a radiation tolerant ASIC. Implementation feasibility was confirmed and the size of the IP core on various chip technologies was estimated.

3.4 STAR Fire

To support the testing of SpaceFibre a suitable test platform was required, so STAR-Dundee Ltd. developed the STAR Fire unit. A block diagram of this unit is illustrated in Fig. 2.

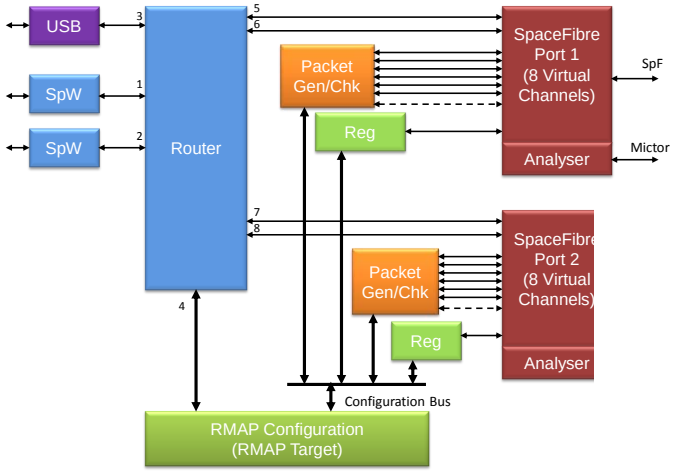

Fig. 2. STAR Fire SpaceFibre Development Kit

The STAR-Fire unit contains two SpaceFibre interface each with eight virtual channels. Two virtual channels of each SpaceFibre interface are connected to a SpaceWire router, which also has two SpaceWire ports, a USB port and an RMAP configuration port. This allows the two SpaceWire interfaces and the USB interface to send packets through either SpaceFibre interface. To test the SpaceFibre interface at full speed and to exercise and validate the bandwidth reservation, priority and scheduled qualities of service, a packet generator and checker is attached to six of the virtual channels of each SpaceFibre interface. The STAR Fire unit is configured and controlled by a Remote Memory Access Protocol (RMAP) interface attached to the SpaceWire router. This allow configuration to be performed over the SpaceWire interfaces, USB interface or the SpaceFibre interfaces. Each SpaceFibre interface has an analyser attached which can be used to record and analyse the operation of the SpaceFibre interface. This was a very important capability during testing of the SpaceFibre IP core and validation of the standard. A graphical user interface provides access to all the capabilities of STAR Fire. An example analysis display is shown in Fig. 3.

Fig. 3. STAR Fire Analysis Display

3.5 VHiSSI

A radiation tolerant SpaceFibre interface device is being developed by University of Dundee and several partners within the Very High Speed Serial Interface (VHiSSI) European Commission Framework 7 project [9]. The VHiSSI project is integrating a complete SpaceFibre protocol engine, together with the physical layer interfaces, in a radiation tolerant chip manufactured by a European foundry. A block diagram

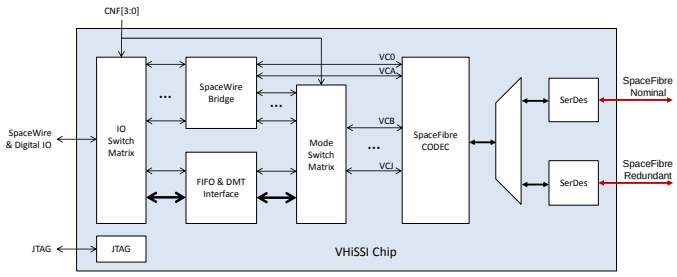

Fig. 4. VHiSSI Chip Block Diagram

There are five main functions within the VHiSSI chip:

- SpaceWire Bridge
- FIFO, DMA, Memory and Transaction Interface
- SpaceFibre Interface
- SerDes
- IO Switch Matrix
- Mode Switch Matrix

The SpaceWire Bridge provides a bridge between SpaceWire and SpaceFibre with up to 11 SpaceWire interfaces being available. The SpaceWire Bridge includes a SpaceWire router which allows routing between the SpaceWire ports and the Virtual Channel (VC) buffers of the two SpaceFibre interfaces. Configuration of the VHiSSI chip can be carried out over any SpaceWire interface connected to the embedded SpaceWire router or over VC0 or VCA of the SpaceFibre interface. The SpaceWire Bridge is connected to the IO Switch Matrix and to the Mode Switch Matrix.

The FIFO and DMA, Memory and Transaction (DMT) Interface provides various types of parallel interface into the VHiSSI chip for sending and receiving data over the SpaceFibre interfaces. The various parallel interface functions have been designed with specific application scenarios in mind and between them are able to operate with many types of local host system, including FPGAs and processors. The parallel interface is also designed to use a small number of pins, so that the VHiSSI chip can fit into a small (100 pin) package

The SpaceFibre Interface has 11 virtual channels. VC 0 is intended primarily for VHiSSI device and local system configuration and monitoring and is connected to the embedded SpaceWire router. The other VCs have programmable VC numbers and so are referred to by letters. VCA is connected to the embedded SpaceWire router. The other VCs are either connected to the

SpaceWire router, directly to a SpaceWire interface, or to the parallel interface, depending on the mode of operation. Each VC supports full SpaceFibre QoS which can be configured independently for each VC. VC0 and VCA are directly connected to the embedded SpaceWire router. The other SpaceFibre VC buffers are connected to the Mode Switch Matrix which connects them to either the SpaceWire Bridge or the parallel interface. The other side of the SpaceFibre interface is connected via a multiplexer to either the nominal or redundant SerDes and CML transceiver.

The SerDes converts parallel data words from the SpaceFibre interface into a serial bit stream and vice versa. On the receive side the bit clock is recovered from the serial bit stream by the SerDes. The SerDes includes integral CML transceivers.

The IO Switch Matrix connects either the SpaceWire LVDS, SpaceWire LVTTL or parallel interface signals from the FIFO and DMT interface to the digital IO pins of the VHiSSI chip. Configuration is static and determined on exit from device reset.

The Mode Switch Matrix connects either the SpaceWire Bridge or FIFO and DMT interface (parallel interface) to the VC buffers of the two SpaceFibre interfaces. Configuration is static and determined on exit from device reset.

3.6 Electrical Connectors and Cable Assemblies

Axon's AxoMach range of connectors and cables are currently baselined for use within SpaceFibre although the specification will allow the use of other types of connector and cable. Within the frame of the ESA SpaceFibre Demonstrator activity Axon will investigate alternative connector configurations and provide an open specification for the cable and connectors. The spaceflight capable AxoMach cable assembly is illustrated in Fig. 5. Laboratory testing has shown that SpaceFibre will operate at a distance of over 5 m using these cables and connectors.

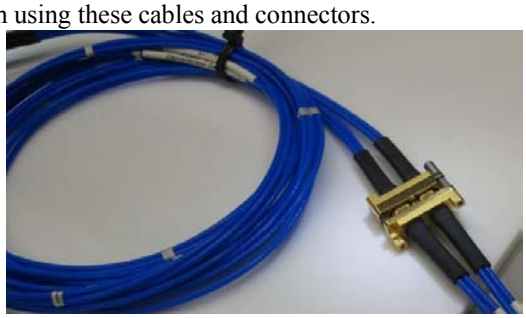

Fig. 5. Prototype SpaceFibre Flight Cable from Axon

3.7 Fibre Optic Transceivers and Cable Assemblies

For longer distances Patria are working for ESA on fibre-optic cables, connectors and transceivers. Tests have been made on prototype fibre-optic devices. In Fig. 6. two STAR Fire units are being used to test SpaceFibre signals running through radiation tolerant fibre optic transceivers and over 100 m fibre optic cable.

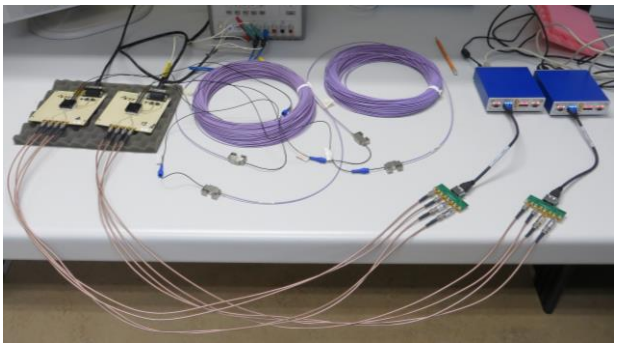

Fig. 6. STAR Fire Testing 100m Fibre Optic Cable

3.8 Beta Test Sites

Several ESA projects are using the Dundee SpaceFibre IP core under a Beta evaluation programme including:

- High Processing Power DSP, Astrium and STAR-Dundee Ltd.
- High Performance COTS Based Computer, Astrium and CGS.
- Leon with Fast Fourier Transform Co-processor, SSBV.
- FPGA Based Generic Module and Dynamic Reconfigurator, Bielefeld University.
- Next Generation Mass Memory, Astrium, IDA and University of Dundee.

Feedback from these beta sites will be used to improve the SpaceFibre standard and the SpaceFibre VHDL IP core and related documentation.

In additional some other organisations are currently testing the Dundee SpaceFibre VHDL IP core for space-based instrumentation interfacing applications.

3.9 Japanese Implementations

NEC and Melco are both developing SpaceFibre interface devices to the specification produced by the University of Dundee. This work has provided valuable feedback on the specification and implementation of SpaceFibre. Interoperability testing in December 2013 and April 2013 has been successful with various levels of the SpaceFibre protocol stack being implemented and tested. Several issues were uncovered during the interoperability testing which resulted in clarifications and errors being resolved in the SpaceFibre standard specification.

3.10 Spaceflight Engineering Model

To raise the TRL of SpaceFibre a spaceflight engineering model is being developed by Astrium in the frame of the ESA SpaceFibre Demonstrator project

[10]. This will use the Dundee IP core integrated with some other interface and test logic in a Microsemi AX2000 FPGA. Texas Instrument TLK2711 devices will be used for the serialisation and de-serialisation. Both devices are available in radiation tolerant, space grade parts. A block diagram of the planned SpaceFibre engineering model is illustrated in Fig. 7. Extensive te th th

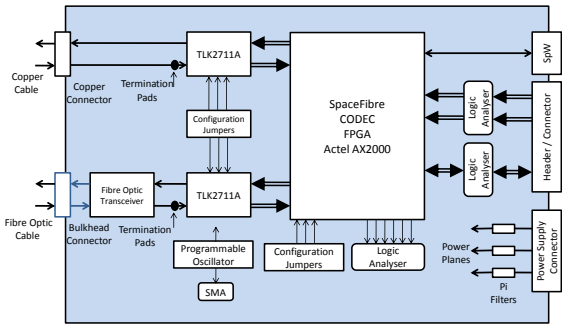

Fig. 7. SpaceFibre Engineering Model

4 CONCLUSIONS

SpaceFibre is a multi-gigabit/s networking technology designed specifically for spaceflight applications. It incorporates a comprehensive quality of service capability providing integrated bandwidth reservation, priority and scheduling. Efficient, effective and rapid fault detection, isolation and recovery mechanisms are included in the SpaceFibre interface, enabling rapid detection and recovery from link level errors.

SpaceFibre has been simulated, implemented and tested extensively in support of the standard specification. Several beta site evaluations of SpaceFibre are underway using the SpaceFibre IP core in various spacecraft applications. Flight connectors and cable for both electrical and fibre-optic media are being developed. A SpaceFibre engineering is currently being developed to raise the TRL of SpaceFibre.

5 ACKNOWLEDGMENTS

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6 REFERENCES

[1] S. Parkes, A. Ferrer and A. Gonzalez, “SpaceFibre Standard”, Draft F3 September 2013, available from http://space-env.esa.int/indico/confLogin.py?confId=32 (last accessed 15th Feb 2014).

[2] S. Parkes, A. Ferrer, A. Gonzalez, & C. McClements, “SpaceFibre: Multiple Gbits/s Network Technology with QoS, FDIR and SpaceWire Packet Transfer Capabilities”, International SpaceWire Conference, Gothenburg, June 2013.

[3] S. Parkes, “Never Mind the Quality, Feel the Bandwidth: Quality of Service Drivers for Future Onboard Communication Networks”, paper no. IAC-10.B2.6.6, 61st International Astronautical Congress, Prague 2010.

[4] S. Parkes, C. McClements and M. Suess, “SpaceFibre”, International SpaceWire Conference, St Petersburg, Russia, 2010, ISBN 978-0-9557196-2-2, pp 41-45.

[5] ECSS Standard ECSS-E-ST-50-12C, “SpaceWire, Links, Nodes, Routers and Networks”, Issue 1, European Cooperation for Space Data Standardization, July 2008.

[6] V. Olenev, I. Lavrovskaya, and I. Korobkov, “SpaceWire-RT/SpaceFibre Specification and Modelling”, International SpaceWire Conference, Gothenburg, 2013.

[7] Brice Dellandrea, Baptiste Gouin, Steve Parkes and David Jameux, “MOST: Modeling of SpaceWire & SpaceFibre traffic”, paper submitted for DASIA 2014.

[8] STAR-Dundee, “SpaceFibre IP Core Data Sheet”, http://www.star-dundee.com/products/spacefibre-ip-core

[9] S. Parkes, A. Ferrer, A. Gonzalez, C. McClements, R. Ginosar, T Liran, G Sokolov, G Burdo, N Blatt, P Rastetter, M Krstic, A Crescenzio, “A Radiation Tolerant SpaceFibre Interface Device”, International SpaceWire Conference, Gothenburg, 2013.

[10] T. Helfers, P. Rastetter, C. Papadas, and S. Parkes, “SpaceFibre Demonstrator (Demonstration and Testing)”, paper submitted for DASIA 2014.