Integrating STAR-Dundee SpaceFibre Codec with TI TLK2711

Onboard Equipment and Software, Short Paper

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***Abstract*—The SpaceFibre Codec IP (beta version) was released by STAR-Dundee at the end of 2013. The SpaceFibre standard and the codec IP are designed in the way that it shall work with TI TLK2711-SP – a space qualified SERDES device [1]. This paper presents the work where the Codec IP and the TLK2711 are used to implement a SpaceFibre link. Firstly the SpaceFibre Codec and the TLK2711 device are introduced, especially the power-on reset and signal detection operations of the TLK2711 for they are fundamental for the SpaceFibre link. Experiments on link initialisation are presented with results and analysis.**

***Index Terms*— SpaceFibre Codec IP, TLK2711, SpaceFibre Link, Link Initialisation**

I. Introduction

SpaceFibre is a very high speed serial communications link which is being designed for use on board spacecraft. As SpaceFibre is compatible with SpaceWire at packet level, a SpaceFibre link can transfer a SpaceWire packet but at a much higher speed. It also provides a broadcast mechanism similar to SpaceWire time-codes but offering much more capability. SpaceFibre is a complementary technology to the currently popular SpaceWire, and applications developed for SpaceWire can be readily transferred to SpaceFibre.

SpaceFibre is designed to have a link speed of 2.5 Gigabits per second, as is achievable with current space qualified technology. It is possible to reach even higher speed, 20 Gigabits per second, with future technology, and multi-laning. Beside the high performance in speed, SpaceFibre has more worthy features, such as low latency, integrated Quality of service (QoS), and integrated FDIR capabilities.

A SpaceFibre Codec VHDL IP core has been developed at STAR-Dundee to evaluate and validate the SpaceFibre standard. A beta version of the Codec IP core was released around the end of 2013. The Codec IP is able to operate with an external SerDes device with minimal glue logics, including the Texas Instruments TLK2711-SP Wizard Link device. Together with a Microsemi Rad-Tolerant RTAX-2000 device, the Codec IP and the TLK2711-SP are ready to build a flight qualified SpaceFibre System.

TLK2711-SP is a Space qualified component, with flight heritages. Its commercial counterpart is TLK2711A, and they are functionally equivalent.

For the HPPDSP (High Processing Power Digital Signal Processor) project, high-speed data I/O interfaces are desired for which the SpaceFibre technology is a perfect fit. Designed for this project, the prototyping board is equipped with a Xilinx Virtex-4 FPGA and three TLK2711A devices, which are used for the implementations of three SpaceFibre interfaces. The STAR-Dundee SpaceFibre Codec IP has been successfully implemented on the FPGA, connected to the TLK2711A devices. Each of the interfaces has a number of virtual channels.

This paper firstly introduces the IP core and the TLK2711 device. Then the integration design is presented. Finally some experimental results are given and analysed.

II. STAR-Dundee SpaceFibre Codec IP

The STAR-Dundee SpaceFibre Codec IP core was developed as part of the standard development for its evaluation and validation. It is in the form of VHDL source codes, and it is highly configurable giving flexibility through generics, such as the number of virtual channels.

The CODEC is organized in layers that are defined in the standard, with interfaces between each layer. It doesn't include the physical and serialisation layers. For the encoding layer, it can be configured to include or exclude the 8B10B encoding/decoding module, or more specifically to have a special interface to the TLK2711 device. This enables the IP core with capability to connect with different technologies.

SpaceFibre Codec can transmit and receive SpaceWire packets encapsulated within Virtual Channel data frames, and also Broadcast frames and control words used to provide the QoS and the FDIR capabilities. This information is passed to the SpaceFibre interface via the Virtual Channel interface, the Broadcast interface, and the Management interface as shown in Fig. 1.

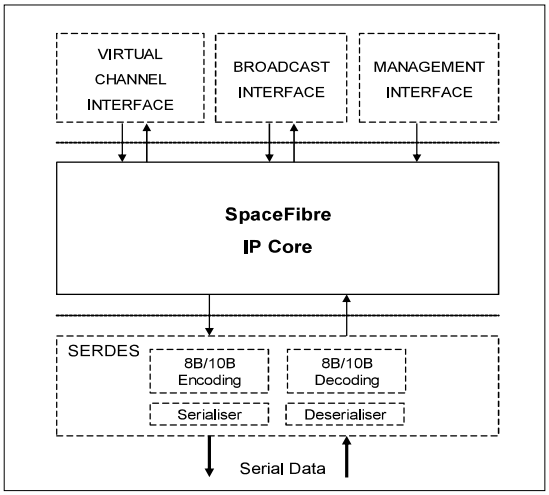

Fig. 1. Overview of STAR-Dundee SpaceFibre Codec IP Core

III. TI TLK2711 Device

The TI TLK2711-SP Wizard Link device is a Space qualified multigigabit transceiver. The device contains both a transmitter and receiver, performing parallel-to-serial and serial-to-parallel data conversion. This device offers data rates from 1.28 to 2.0 Gigabits/s (at a link speed of 1.6 to 2.5 Gigabits/s).

The transmitter takes in 16-bit wide serial data, encodes it using 8B/10B encoding and serialises it for transmission over a VML differential signal pair. The receiver takes the serial data, de-serialises it, and performs 8B/10B decoding to provide the 16-bit parallel data.

A. TLK2711 Transmitter

The parallel data input to the transmitter comprises two bytes of data (TXD0-7 and TXD8-15) along with two control/data flags (TKLSB and TKMSB respectively). The control/data flags are high when the corresponding data byte contains a control code (K-code) and low when it contains data. The two data bytes and the control/data flags are latched into an 18-bit register on the rising edge of the TXCLK signal.

The TXCLK signal must be a continuous clock with a frequency in the range 80 to 125 MHz. It drives most of the transmitter circuits. There is a clock synthesiser which multiplies up TXCLK by 20 to provide the clock to drive the parallel to serial converter. The clock synthesiser also provides a reference clock for the clock recovery circuitry in the receiver.

To mitigate signal degradation on copper transmission media, two levels of pre-emphasis may be selected using the PRE input. When low the pre-emphasis is 5%, when high it is 20%.

The ENABLE signal is normally asserted to allow the TLK2711 device to operate. When de-asserted, the device is put in a power down mode with substantially reduced power consumption, as only signal detection circuit is active which draws less than 15 mW. In the power down mode, the serial transmit pins (TXN), the receiver data bus pins (RXD0-15) and RKLSB are tri-stated. But TXCLK clock still needs to be provided in power-down mode.

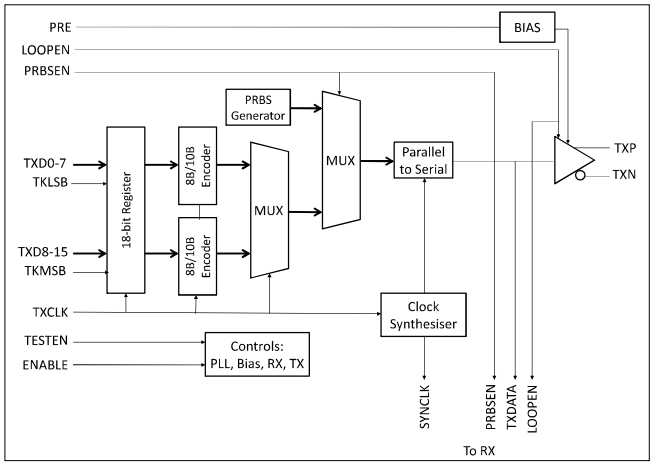

Fig. 2. TLK2711 Transmitter Block Diagram

B. TLK2711 Receiver

The received signal is fed via a pair of multiplexers to a serial to parallel convertor and to an interpolator and clock recovery block. The interpolator and clock recovery block recovers the received clock, to provide bit and word synchronisation. Bit synchronisation is achieved using a phase locked-loop (PLL) that takes the transmit bit clock from the transmitter (SYNCLK) as a reference and provides an output frequency locked to the transitions on the received serial bit stream.

The serial data is converted to a correctly aligned pair of 10-bit codes. The two 10-bit codes are decoded by a pair of 8B/10B decoders, each providing an 8-bit data byte and a control/data flag RKMSB and RKLSB). These signals are registered in an 18-bit register.

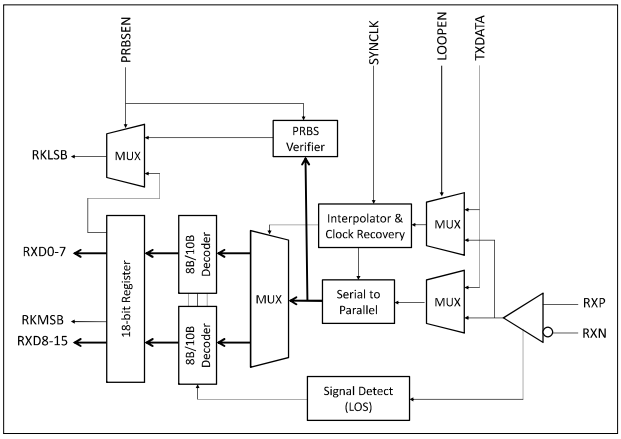

Fig. 3. TLK2711 Receiver Block Diagram

C. Power-on Reset

Upon application of minimum valid power, the device goes through a power-on reset process. When ENABLE pin is asserted high from a power-down mode, the device also goes

into power-on reset process before the normal operation begins.

During power-on reset, RXCLK is held low; the receiver data bus pins (RXD0-15) and RKLSB/RKMSB are in high-impedance state; the serial transmit pins (TXP/TXN) are high impedance as well.

The length of the process depends on the TXCLK frequency, but is less than 1 ms.

D. Loss of Signal (LoS) Detection

Loss-of-Signal detection is intended to be an indication of error conditions like a detached cable or no signal being transmitted, where the incoming signal no longer has sufficient voltage amplitude to keep the clock recovery circuit in lock. When loss of signal is detected the RXD0-15, RKMSB and RKLSB signals are all set high. This represents an invalid K-code on both bytes so can be safely decoded to mean loss of signal.

In power-down mode, the signal detection circuit is still active, and the RKMSB pin indicates the presence or otherwise of a signal on the receiver inputs. This can be used to provide an auto-start capability on a bi-directional serial link (similar to that used for SpaceWire). To save power when there is no data to send or to provide warm redundancy, the link can be put in the power down mode (ENABLE de-asserted).

This signal detection circuit enables the auto-start capability of a SpaceFibre link. When one end of the link has data to send it can enable its TLK2711 device and start sending data. The other end of the link, in power-down mode, detects that there is now a signal on the receiver inputs (RKMSB goes HIGH indicating that there is no longer loss-of-signal). The TLK2711 device at that end of the link can then be enabled and the link begins normal operation.

IV. SpaceFibre Interfaces on HPPDSP

HPPDSP project requires the I/O data interfaces having a very high speed, for which the SpaceFibre technology has been adopted. There are three SpaceFibre ports on a HPPDSP prototyping board. For each port, there is a double-deck eSATA connector as shown in Fig. 4. The upper deck is connected to MGT RocketIO on the Xilinx Virtex-4 FPGA. The lower deck is connected to a TLK2711 device. For this project, the lower decks are in use.

Fig. 4. Picture of SpaceFibre Ports on HPPDSP Unit

For each SpaceFibre interface, there are a number of virtual channels (VC), for instance four VCs (VC0 – VC3). The VC0, connected to a RMAP Target (and a RMAP initiator on one interface), is used to access the Configuration Bus on the FPGA design for configuration and control purpose. The VC1, VC2 and VC3 are connected to the IO DMA bus for data I/O transmission at high speed.

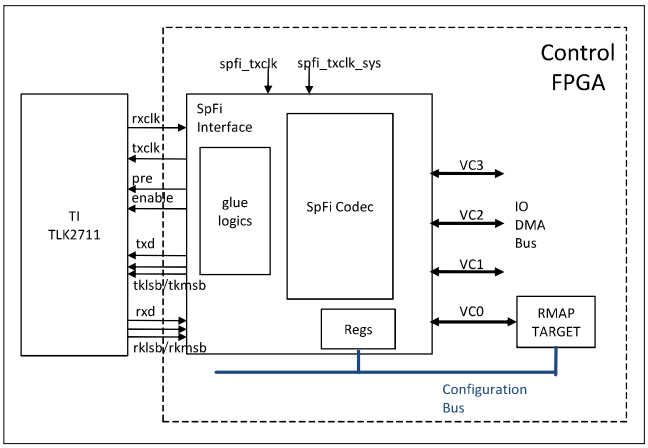

Fig. 5. Block Diagram of SpaceFibre Interface on HPPDSP

V. Experiments

Two HPPDSP prototyping boards are used for the experiments. The SpaceFibre interfaces can be configured to "Disabled", "Start", or "Auto-Start", using the Configuration Bus.

A. Loss of Signal (LoS) Detection

This experiment checks the operations of the signal detection circuit, under circumstances of forced no-signal and forced signal on the link.

The no-signal scenario is simulated with cable unplugged. When the TLK2711a device is enabled, the receiver outputs K31.7 on both MSB and LSB. When the device is disabled, the RK_MSB is set low.

After the rising edge of the ENABLE pin, the outputs by the receiver are not reflecting the true state, as shown in Fig. 6. One can see a short false-positive pulse on the signal detection, which is about 6.2 us. It is rational to conclude this is due to the power-on reset process.

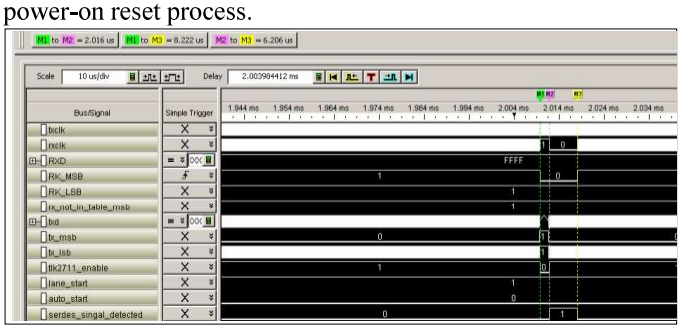

Fig. 6. Signal Detection with Forced No-signal Scenario

The forced signal scenario is simulated with the other end of the link set to "Start". When the TLK2711a device is enabled, the receiver doesn't outputs K31.7 on both MSB and LSB. When the device is disabled, the RK_MSB is set high. After the falling edge of the ENABLE pin, one can see a short low pulse on the signal detection in Fig. 7. This is because the simulated scenario is not perfect, and for that period the other end of the link was going through a reset cycle.

Fig. 7. Signal Detection with Forced Signal Scenario

B. Link Initialisation

An eSATA cable connects a SpaceFibre interface on one board to a SpaceFibre interface on the other board. This experiment has six different test cases. For each one, the same test is carried out three times. The time taken for this end to connect is recorded.

TABLE I. TEST CASES FOR EXPERIMENTS ON LINK INITIALISATION

Case	*This End*	*Remote End*	*Time to Connect*
1	Then Start	Started	~40us
2	Then Auto-Start	Started	~40us
3	Started	Then Start	~35us after receiving first signal
4	Started	Then Auto-Start	~35us after receiving first signal
5	Then Start	Auto-Started	~53us
6	Auto-Started	Then Start	~53us after receiving first signal

Test Case 1 and Test Case 2 are essentially the same test. Test Case 3 and Test Case 4 are essentially the same test. When one end is started, it tries to connect so it sends signal which can be picked up by the other end. Therefore "Then Start" and "Then Auto-Start" are not making any difference.

For Test Case 1, before this end is set to "Start", signal has been detected on the link. As soon as this end is set to "Start" at marker M1 in Fig. 8, the TLK2711 device is enabled.

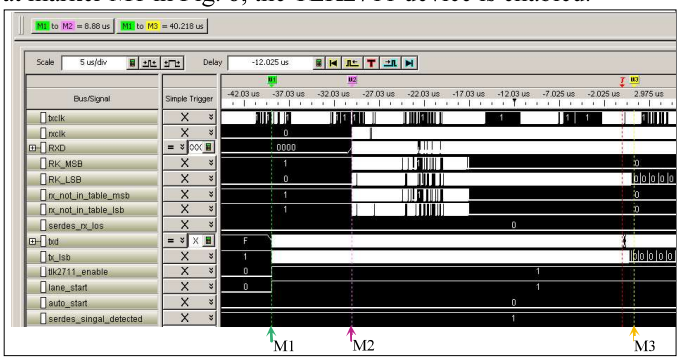

Fig. 8. Link Initialisation under Test Case 1

Then the power-on reset is in process, until there is the RXCLK at marker M2 in Fig. 8. Following that, it takes some further time for the device to synchronise and lock with the incoming serial data and to find a comma to align on the word boundary. Then it takes about 18us for the SpaceFibre Lane initialisation state machine to go through various states and get connected. In Fig. 8, the point that the link is connected is at maker M3, where it starts to send out IDLE frames.

For Test Case 3, this end has been started, and the TLK2711 device has been enabled. It is at marker M1 in Fig. 9 when the first signal is received. After about 16us, the device synchronised and locked with the incoming serial data and found a comma to align on the word boundary. Then it takes another about 18us for the link to get connected at maker M3 where it starts to send out IDLE frames.

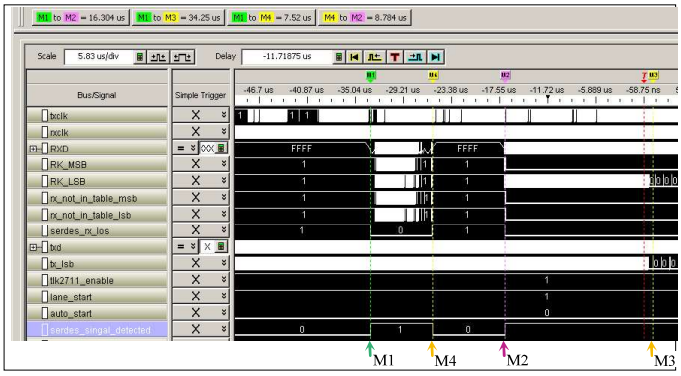

Fig. 9. Link Initialisation under Test Case 3

For Test Case 6, this end has been set to Auto-Start. The TLK2711 device is enabled as soon as signal detected on the link that is at marker M1 in Fig. 10. After going through the power-on reset process, at yellow marker M4, it detects a LoS and therefore the TLK2711 device is disabled. At marker M2, signal is detected again and so the TLK2711 device is enabled. Then similarly it takes 16us plus 18us for the link to get connected at maker M3. The reason for the LoS detected may due to the remote end was in the power-on reset process.

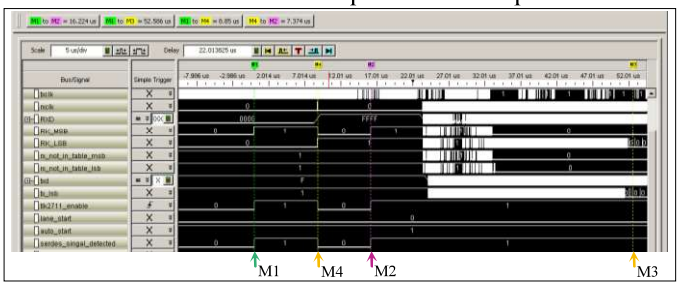

Fig. 10. Link Initialisation under Test Case 6

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REFERENCES

[1] S. Parkes, and C. McClements, "SPACEFIBRE CODEC: USE OF THE TLK2711-SP," Proceedings of the 4th International SpaceWire Conference, San Antonio, 2011

[2] S. Parkes, A. Ferrer, A. Gonzalez, and C. McClements, "SpaceFibre Specification Draft F1", May 2013

[3] Texas Instruments, "TLK2711-SP Data Sheet: 1.6-Gbps to 2.5-Gbps Class V Transceiver", Reference Number SGLS307D, July 2006, Revised July 2009.