SpaceFibre Implementation, Test and Validation

SpaceFibre, Long Paper

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***Abstract*—SpaceFibre is a multi-gigabit/s data link and network technology for use onboard spacecraft. Compatible with SpaceWire at the packet level, SpaceFibre runs over electrical and optical media. It provides extensive quality of service (QoS) and fault detection, isolation and recovery (FDIR) capabilities that are designed specifically for spacecraft applications. This paper provides a short introduction to SpaceFibre and then describes how SpaceFibre is being implemented. It introduces some SpaceFibre test equipment and explains how SpaceFibre has been validated. SpaceFibre is designed to support high data rate payload data-handling like synthetic aperture radar (SAR), multi-spectral imaging systems and fast mass memory. It is an ideal candidate for the next generation of spacecraft interconnect, being an open standard designed specifically for spacecraft applications.**

***Index Terms*—SpaceWire, SpaceFibre, Network, Spacecraft Onboard Data-Handling, Quality of Service, FDIR, Next Generation Interconnect.**

I. Introduction

SpaceFibre [1][2][3] is a very high-speed serial data-link being developed by the University of Dundee for ESA for use with high data-rate payloads. The draft SpaceFibre standard has been written by the University of Dundee for ESA and has been reviewed by the international spacecraft engineering community. It has also been simulated and implemented in several forms. SpaceFibre is currently being integrated into several third party beta test applications to help refine the standard.

The SpaceFibre standard is described in section II. The design of a SpaceFibre IP core is outlined in section III. A radiation ASIC implementation of SpaceFibre is described in section IV. Currently available test equipment and future test equipment for SpaceFibre is considered in section V. The ways in which the SpaceFibre standard has been validated are explained in section VI.

II. The SpaceFibre Standard

SpaceFibre is currently a draft standard being specified by the University of Dundee with contributions from several other organisations. The protocol stack for SpaceFibre is illustrated in Fig. 1.

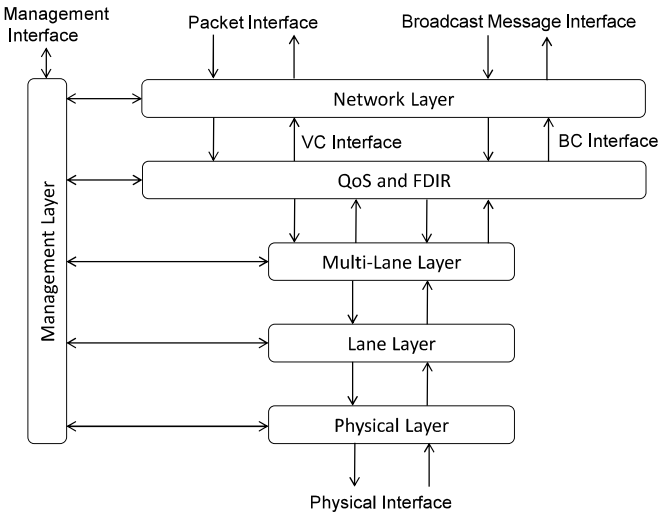

Fig. 1. SpaceFibre Protocol Stack

The network layer protocol provides two services for transferring application information over a SpaceFibre network; the packet transfer service and the broadcast message service. The Packet Transfer Service transfers SpaceFibre packets over the SpaceFibre network, using the same packet format and routing concepts as SpaceWire. The broadcast message service broadcasts short messages carrying time and synchronisation information to all nodes on the network.

The QoS and FDIR layer provides quality of service and flow control for a SpaceFibre link. It frames the information to be sent over the link to support QoS and scrambles the packet data to reduce electromagnetic emissions. It also provides a retry capability; detecting any frames or control codes that go missing or arrive containing errors and resending them.

The Multi-Lane layer is able to operate several SpaceFibre lanes in parallel to provide higher data throughput. In the event of a lane failing the Multi-Lane layer provides support for graceful degradation, automatically spreading the traffic over the remaining working links. It does this rapidly without any external intervention.

The Lane layer initialises each lane initialisation and re-initialises the lane when an error is detected. Data is encoded into symbols for transmission using 8B/10B encoding and

decodes these symbols in the receiver. 8B/10B codes are DC balanced supporting AC coupling of SpaceFibre interfaces.

The Physical layer serialises the 8B/10B symbols and sends them over the physical medium. In the receiver the Physical layer recovers the clock and data from the serial bit stream, determines the symbol boundaries and recovers the 8B/10B symbols. Both electrical cables and fibre-optic cables are supported by SpaceFibre.

The management layer supports the configuration, control and monitoring of all the layers in the SpaceFibre protocol stack.

The SpaceFibre standard has been simulated, implemented and reviewed at all stages of its research, design and development. The lane and QoS layers of SpaceFibre are fully defined and have been extensively tested with simulations by at least three independent organisations, and by implementation in FPGAs. The physical layer is well on the way to being complete with final inputs on eye pattern masks etc. to be added. The multi-lane layer has been designed and simulated, and is currently in the process of being implemented and tested in FPGAs. Once this testing is complete and the specification updated to resolve any issues found, draft G of the SpaceFibre standard will be issued and an ECSS working group will be convened to finalise the standard for formal approval.

The SpaceFibre network layer will be a separate standard document. The network layer uses the same packet format as SpaceWire and supports path and logical addressing.

III. A SpaceFibre IP Core

A SpaceFibre IP core has been designed and developed to test and validate the SpaceFibre specification. This has been updated and used to re-validate each revision of the SpaceFibre standard. A block diagram showing the interfaces to the IP Core is given in Fig. 2. The current version SpaceFibre IP core is complaint to draft F3 version of the SpaceFibre standard and supports all its features with the exception of multi-laning.

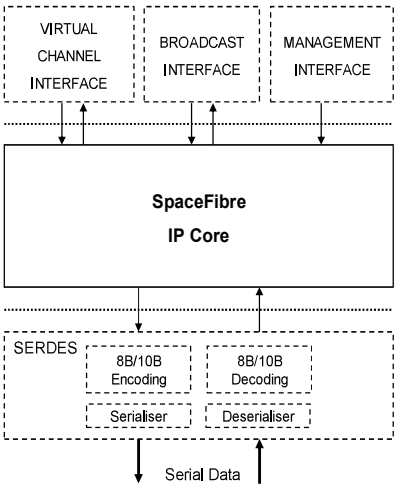

Fig. 2. SpaceFibre IP Core Interfaces

The SpaceFibre IP Core is designed to interface with an 8B/10B encoder/decoder and SerDes. This allows the SpaceFibre IP Core to be used with space qualified SerDes such as the TLK2711-SP device from Texas Instruments. The application interface to the SpaceFibre IP core comprises three separate interfaces:

1. A virtual channel interface, which is used to send and receive SpaceFibre packets over the virtual channels in the interface.
2. A broadcast interface, which is used to send broadcast messages over the SpaceFibre network.
3. A management interface, which is used to configure, control and monitor the status of the SpaceFibre interface.

The FPGA resources required for a SpaceFibre link with a single virtual channel are detailed for various types of space qualified, radiation tolerant FPGAs in Fig. 3. to Fig. 5. The utilisation for an 8 virtual channel interface is about twice that of a single virtual channel interface.

```
************************************************************
Device Utilization for XQR4VLX200CF1509
************************************************************
Resource                          Used    Avail   Utilization
------------------------------------------------------------
IOs                               618     -           -
Global Buffers                    0       32        0.00%
LUTs                              4299    89088     4.83%
CLB Slices                        2150    89088     2.41%
Dffs or Latches                   2525    178176    1.42%
Block RAMs                        5       336       1.49%
   RAMB16                         5
Distributed RAMs
   RAM16X1D                       67
DSP48s                            1       96        1.04%
------------------------------------------------------------
```

Fig. 3. SpaceFibre Single Virtual Channel Xilinx Virtex 4 FPGA Utilisation

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************************************************************
Device Utilization for XQ5VLX330TEF1738
************************************************************
Resource                          Used    Avail   Utilization
------------------------------------------------------------
IOs                               618     -           -
Global Buffers                    0       32        0.00%
LUTs                              3331    207360    1.61%
CLB Slices                        833     51840     1.61%
Dffs or Latches                   2523    207360    1.22%
Block RAMs                        3       324       0.93%
   RAMB18                         1
   RAMB18SDP                      4
Distributed RAMs
   RAM32M                         13
DSP48Es                           1       192       0.52%
------------------------------------------------------------
```

Fig. 4. SpaceFibre Single Virtual Channel Xilinx Virtex 5 FPGA Utilisation

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************************************************************
Device Utilization for RTAX2000S/256CQFP
************************************************************
Resource                          Used    Avail   Utilization
------------------------------------------------------------
IOs                               618     -           -
Modules                           7804    32256    24.19%
Sequential modules                2691    10752    25.03%
Combinational modules             5113    21504    23.78%
Global HCLKs                      0       4         0.00%
Global RCLKs                      0       4         0.00%
RAM Blocks                        9       64       14.06%
Mathblocks                        0       0         0.00%
------------------------------------------------------------
```

Fig. 5. SpaceFibre Single Virtual Channel Microsemi RTAX2000 Utilisation

The SpaceFibre IP core has been designed to support the testing of the SpaceFibre standard. It has not been designed for

speed or size. A version of the SpaceFibre IP core targeted for high performance and small size in flight qualified FPGAs is currently being developed by STAR-Dundee Ltd. This IP core is designed to support instrument interfacing with SpaceFibre using existing flight proven FPGAs and SerDes devices.

IV. A Radiation Tolerant SpaceFibre Device

A radiation tolerant SpaceFibre interface device has been developed by University of Dundee, STAR-Dundee, Ramon Chips, ACE-IC, IHP, Airbus DS and SCI within the Very High Speed Serial Interface (VHiSSI) European Commission Framework 7 project [5]. The VHiSSI chip integrates a complete SpaceFibre protocol engine, together with the physical layer interfaces, in a radiation tolerant chip manufactured by a European foundry. A block diagram of The VHiSSI device is shown in Fig. 6.

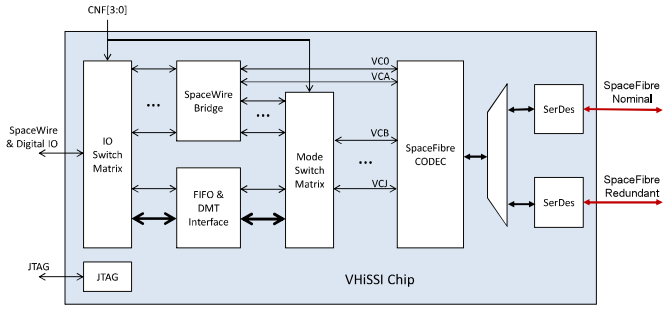

Fig. 6. VHiSSI Chip Block Diagram

There are five main functions within the VHiSSI chip:

- SpaceWire Bridge
- FIFO, DMA, Memory and Transaction Interface
- SpaceFibre Interface
- SerDes
- IO Switch Matrix
- Mode Switch Matrix

The SpaceWire Bridge provides a bridge between SpaceWire and SpaceFibre with up to 11 SpaceWire interfaces being available. The SpaceWire Bridge includes a seven port SpaceWire router which allows routing between three SpaceWire ports, three Virtual Channel (VC) buffers of the two SpaceFibre interfaces and a device configuration port. Configuration of the VHiSSI chip can be carried out over any SpaceWire interface connected to the embedded SpaceWire router or over VC0, VCA and VCB of the SpaceFibre interface. The SpaceWire Bridge is connected to the IO Switch Matrix and to the Mode Switch Matrix.

The FIFO and DMA, Memory and Transaction (DMT) Interface provides various types of parallel interface into the VHiSSI chip for sending and receiving data over the SpaceFibre interfaces. The various parallel interface functions have been designed with specific application scenarios in mind and between them are able to operate with many types of local host system, including FPGAs and processors. The parallel interface is also designed to use a small number of pins, so that the VHiSSI chip can fit into a small (100 pin) package

The SpaceFibre Interface has 11 virtual channels. VC 0 is intended primarily for VHiSSI device and local system configuration and monitoring and is connected to the embedded SpaceWire router. The other VCs have programmable VC numbers and so are referred to by letters. VCA and VCB are connected to the embedded SpaceWire router. The other VCs are connected directly to a SpaceWire interface, or to the parallel interface, depending on the mode of operation. Each VC supports full SpaceFibre QoS which can be configured independently for each VC.

VC0 and VCA are directly connected to the embedded SpaceWire router. The other SpaceFibre VC buffers are connected to the Mode Switch Matrix which connects them to either the SpaceWire Bridge or the parallel interface. The SpaceFibre interface is connected via a multiplexer to either the nominal or redundant SerDes and CML transceiver.

The SerDes converts parallel data words from the SpaceFibre interface into a serial bit stream and vice versa. On the receive side the bit clock is recovered from the serial bit stream by the SerDes. The SerDes includes integral CML transceivers.

The IO Switch Matrix connects either the SpaceWire LVDS, SpaceWire LVTTL or parallel interface signals from the FIFO and DMT interface to the digital IO pins of the VHiSSI chip. Configuration is static and determined on exit from device reset.

The Mode Switch Matrix connects either the SpaceWire Bridge or FIFO and DMT interface (parallel interface) to the VC buffers of the two SpaceFibre interfaces. Configuration is static and determined on exit from device reset.

The digital logic for VHiSSI was designed by STAR-Dundee Ltd. with system architectural design and project management being carried out by University of Dundee. AirbusDS provided inputs to the VHiSSI requirements. The back end design was carried out by Ramon Chips. ACE-IC designed the SerDes parts of the chip. Test vectors were prepared by STAR-Dundee and SCI with inputs from other partners. The chip was manufactured by IHP. The resulting VHiSSI chip is shown in Fig. 7.

Fig. 7. VHiSSI SpaceFibre Chip

Initial testing of all chips was carried out at IHP with support from STAR-Dundee and SCI. The VHiSSI chip can be seen on the right hand side of Fig. 8. mounted on a chip tester.

Fig. 8. VHiSSI in Chip Tester at IHP

The chip tester was able to carry out basic testing of the VHiSSI chip, but full-speed functional testing had to be carried out using dedicated test boards and test equipment. Four test boards were designed:

1. SpaceWire LVDS test board, for testing VHiSSI in the SpaceWire bridge mode with five LVDS SpaceWire interfaces and one LVTTL interface. This board is also being used for SEU radiation testing of VHiSSI.
2. SpaceWire LVTTL test board, for testing the SpaceWire bridge mode with eleven SpaceWire LVTTL interfaces.
3. FMC interface test board, for testing the parallel, FIFO and DMT, interface modes of operation.
4. Radiation test board, for testing the total ionising dose characteristics of the VHiSSI device.

A block diagram of the SpaceWire LVDS test board is shown in Fig. 9.

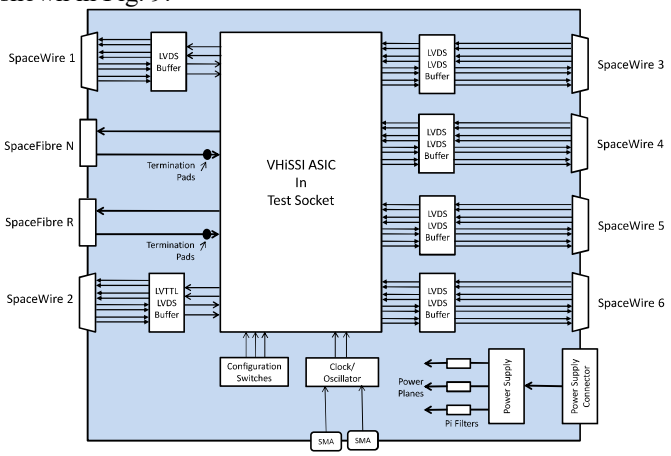

Fig. 9. Block Diagram of VHiSSI SpaceWire LVDS Test Board

The VHiSSI chip is mounted in a specially designed wide bandwidth test socket which can support the SpaceFibre 2.5 Gbits/s serial data rate. The VHiSSI chip is directly connected to the nominal and redundant SpaceFibre interfaces. The SpaceWire interfaces are connected via LVDS buffers to SpaceWire micro-miniature D-type connectors. The LVDS buffers on the board are only necessary for SpaceWire interface 1 which has an LVTTL interface to the VHiSSI chip. The others are there simply to protect the VHiSSI chip during testing since in the SpaceWire LVDS mode they have LVDS interfaces on the VHiSSI chip. A crystal oscillator, configuration switches and power supply circuitry are included on the test board. Latch up protection circuitry is also included within the power supply circuitry for the SEE radiation testing.

The VHiSSI chip was tested using a STAR-Dundee STAR Fire unit, to send and receive SpaceFibre packets and broadcast codes from VHiSSI and to monitor the link during lane initialization and error recovery operations. The STAR-Fire unit is described in section V.

The block diagram of the VHiSSI SpaceWire LVDS illustrates how simple it is to build a SpaceWire to SpaceFibre bridge using the VHiSSI chip, with very few additional components being required especially when external LVDS buffers are not used.

A photograph of the VHiSSI SpaceWire LVDS test board is shown in Fig. 10.

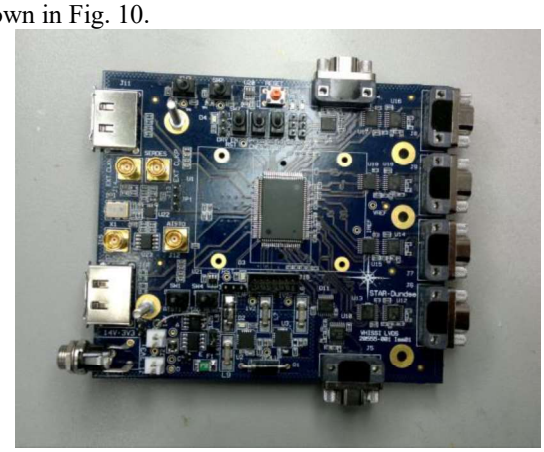

Fig. 10. VHiSSI SpaceWire LVDS Test Board

The radiation test board for VHiSSI is shown in Fig. 11.

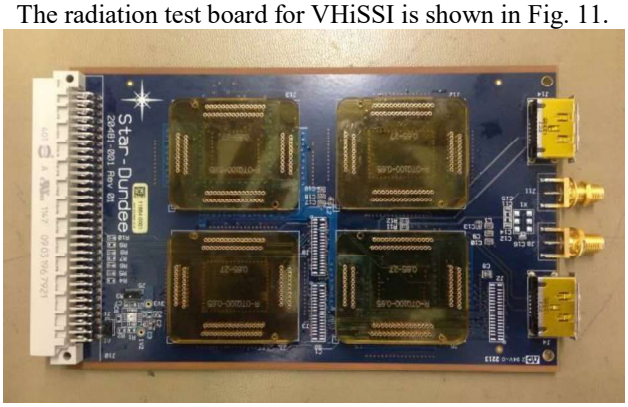

Fig. 11. VHiSSI Radiation Test Board

Four chips are tested together two powered and two not powered with one of the powered devices also clocked.

The VHiSSI chip is currently being tested in Dundee. Initial results from the testing will be available by the end of

September 2014. Radiation testing will be carried out by Airbus DS GmbH in October 2014.

V. SpaceFibre Test Equipment

STAR-Dundee has developed a range of SpaceFibre test and development equipment. The first unit, STAR Fire, was designed to support the testing of SpaceFibre and include SpaceWire to SpaceFibre bridging, pattern generation and checking for multiple virtual channels and link analysis capabilities. A block diagram of STAR Fire is shown in Fig. 12. and a photograph in Fig. 13.

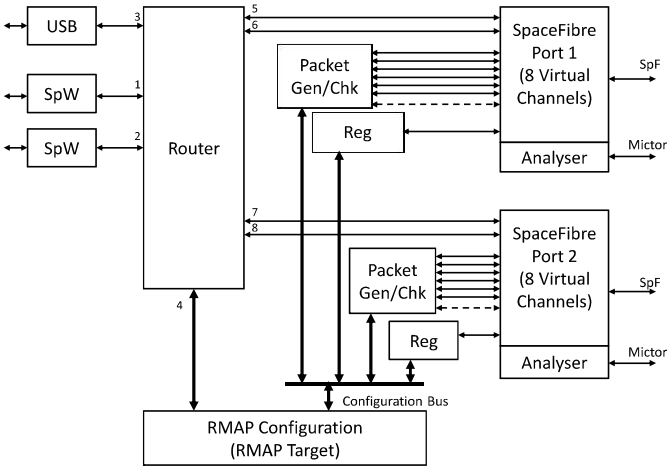

Fig. 12. STAR Fire SpaceFibre Development Kit

The STAR-Fire unit contains two SpaceFibre interface each with eight virtual channels. Two virtual channels of each SpaceFibre interface are connected to a SpaceWire router, which also has two SpaceWire ports, a USB port and an RMAP configuration port. This allows the two SpaceWire interfaces and the USB interface to send packets through either SpaceFibre interface. To test the SpaceFibre interface at full speed and to exercise and validate the bandwidth reservation, priority and scheduled qualities of service, a packet generator and checker is attached to six of the virtual channels of each SpaceFibre interface. The STAR Fire unit is configured and controlled by a Remote Memory Access Protocol (RMAP) interface attached to the SpaceWire router. This allow configuration to be performed over the SpaceWire interfaces, USB interface or the SpaceFibre interfaces. Each SpaceFibre interface has an analyser attached which can be used to record and analyse the operation of the SpaceFibre interface.

Fig. 13. STAR Fire Unit

A graphical user interface provides access to all the capabilities of STAR Fire. Part of an example analysis display is shown in Fig. 14. where the control words being exchanged in each direction are shown in colour and the four symbols that make up the left hand control code being shown in black and white.

ComaInit	LLCW	INIT3	0	INIT3	INIT2
ComaInit	LLCW	INIT3	0	INIT3	INIT2
ComaInit	LLCW	INIT3	0	INIT3	INIT2
ComaInit	LLCW	INIT3	0	INIT3	INIT2
ComaInit	LLCW	INIT3	0	INIT3	INIT3
ComaInit	LLCW	INIT3	0	INIT3	INIT3
ComaInit	LLCW	INIT3	0	INIT3	INIT3
ComaInit	LLCW	INIT3	0	INIT3	INIT3
ComaInit	LLCW	INIT3	0	INIT3	IDLE
ComaInit	LLCW	INIT3	0	INIT3	IDLE
ComaInit	LLCW	INIT3	0	INIT3	IDLE
ComaInit	LLCW	INIT3	0	INIT3	IDLE
ComaInit	LLCW	INIT3	0	INIT3	FCT +1 (1)
ComaInit	LLCW	INIT3	0	INIT3	FCT +2 (2)
ComaInit	LLCW	INIT3	0	INIT3	FCT +3 (3)
ComaInit	LLCW	INIT3	0	INIT3	FCT +4 (4)

Fig. 14. STAR Fire Analysis Display

A cPCI interface board has also been developed for SpaceFibre which is compatible with cPCI, RASTA and National Instruments PXI systems. This board can provide a number of different SpaceFibre functions including SpaceFibre interface, SpaceWire to SpaceFibre bridging and SpaceFibre Router functions. This board is expected to be available early in 2015. The STAR Fire unit is currently available from STAR-Dundee along with the SpaceFibre IP core.

VI. SpaceFibre Validation

The University of Dundee designed the lane layer of SpaceFibre with funding from ESA under the SpaceFibre contract, and the QoS and FDIR layer with funding from the European Commission (EC) SpaceWire-RT grant. The physical, multi-lane and management layers are currently being specified with ESA funding under the SpaceWire Demonstrator contract.

As SpaceFibre was being designed by the University of Dundee, various alternative designs were simulated to rapidly explore alternative designs and support design trade-offs.

In parallel with specifying the SpaceFibre standard the University of Dundee designed and tested the SpaceFibre IP core in VHDL. This was used to validate each revision of the SpaceFibre standard in a series of FPGA implementations.

To support the testing of SpaceFibre a suitable test platform was required, so STAR-Dundee Ltd. developed the STAR Fire unit. This device was used as a validation platform for the SpaceFibre IP core. Link analysis capability was included so that the exchange of information over the SpaceFibre interface could be recorded and analysed.

As the specification of the SpaceFibre standard developed formal simulations of the standard were carried out by St Petersburg University of Aerospace Instrumentation (SUAI), covering drafts C, D and E [6], and by Thales Alenia Space France, covering draft F3. These simulations identified many issues with the SpaceFibre standard which were then rectified.

NEC and Melco in Japan are both developing SpaceFibre interface devices to the specification produced by the University of Dundee. This work has provided valuable feedback on the specification and implementation of SpaceFibre.

Several ESA projects are using the Dundee SpaceFibre IP core under a Beta evaluation programme. Feedback from these beta sites has been used to improve the SpaceFibre standard and the SpaceFibre VHDL IP core and related documentation.

To raise the TRL of SpaceFibre a spaceflight engineering model is being developed by Airbus Defence and Space in the frame of the ESA SpaceFibre Demonstrator project. This design uses already flight proven components (RTAX2000 and TLK2711-SP).

The VHiSSI radiation tolerant SpaceFibre interface device was developed by University of Dundee and partners within the Very High Speed Serial Interface (VHiSSI) European Commission Framework 7 project. This device has been manufactured and is currently being tested.

Axon is working on an open specification for SpaceFibre cable and connectors, which has been referred to in the current draft specification of the SpaceFibre standard. The cables and connectors have been tested using the STAR Fire unit.

VII. Conclusions

SpaceFibre is a multi-Gigabit/s data link and network technology specifically designed for spaceflight applications. It is targeted primarily at spacecraft onboard payload data-handling applications. It includes built in, very efficient, quality of service and fault detection, isolation and recovery techniques, which simplify the use of SpaceFibre enormously; providing substantial system level benefits without requiring the implementation of complex performance limiting software protocols. SpaceFibre is backwards compatible with SpaceWire at the packet level allowing easy bridging between SpaceWire and SpaceFibre, so that existing SpaceWire devices can be incorporated into a SpaceFibre network and take advantages of its performance and QoS and FDIR capabilities.

SpaceFibre has been designed, reviewed and validated through analysis, simulation and hardware implementation, in a series of stages with feedback from each validation cycle feeding into the design. This has resulted in a mature well tested standard which will be released to ECSS for formal standardisation at the end of 2015. The TRL is already at TRL 5 with an implementation designed in flight proven radiation tolerant FPGA and SerDes devices. It will be raised to TRL 6 with application demonstrations in the near future. An experimental radiation tolerant SpaceFibre interface has been designed and manufactured and is currently undergoing tests.

Acknowledgment

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