SpaceFibre Flight Equipment

SpaceFibre, Long Paper

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***Abstract*— SpaceFibre is a new standard for spacecraft on-board data-handling networks, which runs over both electrical and fibre optic media. It provides high bandwidth, low latency, fault recovery and novel QoS that combines priority, bandwidth reservation and scheduling. SpaceFibre is backwards compatible with SpaceWire at the network level, allowing existing SpaceWire equipment to be incorporated into a SpaceFibre network without modification. SpaceFibre is now being designed into its first spaceflight missions. This paper describes SpaceFibre flight equipment being designed by STAR-Dundee for space flight applications. This includes a range of SpaceFibre IP cores targeted at radiation tolerant FPGAs and the SpaceFibre interfaces in a radiation tolerant many core DSP processor.**

***Index Terms* — SpaceFibre, SpaceWire, Flight Equipment, Networking, Spacecraft Electronics.**

I. Introduction

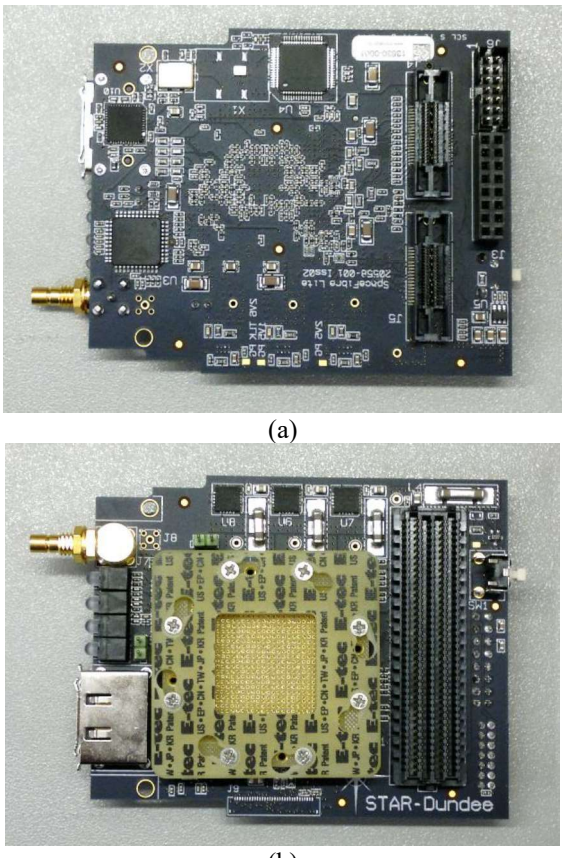
SpaceFibre [1][2][3] is a new standard for spacecraft on-board data-handling networks, initially designed to deliver multi-Gbit/s data rates for synthetic aperture radar and high-resolution, multi-spectral imaging instruments. The addition of quality of service (QoS) and fault detection, isolation and recovery (FDIR) capabilities to SpaceFibre has resulted in a unified network technology. SpaceFibre provides high bandwidth, low latency, fault isolation and recovery suitable for space applications, and novel QoS that combines priority, bandwidth reservation and scheduling and which provides babbling node protection [4]. SpaceFibre is backwards compatible with the widely used SpaceWire standard [5] at the network level allowing simple interconnection of existing SpaceWire equipment to a SpaceFibre link or network.

This paper describes SpaceFibre equipment being designed by STAR-Dundee for space flight applications. This includes a range of SpaceFibre IP cores targeted at radiation tolerant FPGAs, the SpaceFibre interfaces in a radiation tolerant many core DSP processor and boards, subsystems and instrument processing units, containing these devices.

II. SpaceFibre Interface in the RTAX FPGA

A version of the SpaceFibre IP core targeted for high performance and small size in flight qualified FPGAs is currently being developed by STAR-Dundee Ltd. This IP core is designed to support instrument interfacing with SpaceFibre using existing flight proven FPGAs and SerDes devices. It is expected that this design will reduce the size of the SpaceFibre IP core for instrument interfaces significantly.

A board that implements this "SpaceFibre-Lite" IP core in a Microsemi AX1000 FPGA is illustrated in Figure 1.



(a)

(b)

Figure 1. SpaceFibre-Lite board for Microsemi AX1000 FPGA; (a) top-side and (b) bottom-side

On the bottom side of the SpaceFibre-Lite board is a socket for an AX1000 FPGA, which is the commercial equivalent of the radiation tolerant RTAX1000 FPGA [6]. This FPGA does

not include a SerDes so an external SerDes device is required. Texas Instruments have a suitable radiation tolerant SerDes device: the TLK2711-SP Wizard Link device [7]. This device contains both a transmitter and receiver and offers data rates from 1.28 to 2.0 Gbits/s (1.6 to 2.5 Gbits/s data signalling rates). The transmitter takes in 16-bit wide serial data, encodes it using 8B/10B encoding and serialises it for transmission over a differential signal pair. The receiver takes the serial data, de-serialises it, and performs 8B/10B decoding to provide the 16-bit parallel data. The TLK2711A (commercial version) can be seen on the top-side of the board, at the top of Figure 1.

The SpaceFibre-Lite interface has two virtual channels and a broadcast message interface. One virtual channel is used for sending or receiving high data-rate application data, which requires substantial link bandwidth. The other virtual channel is used for receiving configuration, control and housekeeping requests from a remote computer and for returning status and housekeeping information. This latter virtual channel is typically set to high priority, but uses little bandwidth.

The SpaceFibre-Lite board has an FMC connector for connecting to a host system, e.g. another FPGA development board. A 32-bit interface is provided on this FMC connector for sending and receiving data between the host system and the SpaceFibre virtual channels in the AX1000 FPGA. This interface can also be used for configuring the SpaceFibre interface and for accessing the broadcast message interface. For test purposes, a pair of Mictor connectors are provided on the parallel interface to the FMC connector for connection to a logic analyser.

The SpaceFibre serial interface is connected to an eSATA connector which is used in SpaceFibre electrical ground support equipment. This connector can be seen on the bottom left of Figure 1 (b).

All of the major components on the SpaceFibre-Lite board are commercial equivalents of radiation tolerant, spaceflight grade components. It operates at a data signalling rate of 2.5 Gbits/s and demonstrates that SpaceFibre is at TRL5, ready to fly.

III. SpaceFibre in the RTG4 FPGA

The Microsemi RTG4 is a new generation radiation tolerant FPGA [8]. It has extensive logic, memory, DSP blocks, and IO capabilities and is inherently radiation tolerant, having triple mode redundancy built in. The RTG4 has a flash configuration memory built into the device. In addition the FPGA incorporates 16 SpaceWire clock-data recovery circuits and 24 multi-Gbits/s SerDes lanes to support high-speed serial protocols like SpaceFibre. The integrated radiation tolerant SerDes make the RTG4 ideal for the implementation of SpaceFibre.

A SpaceFibre interface has been implemented in the RTG4 FPGA and tested extensively [9]. The test design incorporates two SpaceFibre interfaces and four SpaceWire interfaces. One SpaceFibre interface has eight virtual channels and the other has four. These two SpaceFibre interfaces are connected back to back with VC4-7 on one interface connected to VC4-7 on the other interface. The four SpaceWire interfaces are connected to VC0-3 on the SpaceFibre interface with eight virtual channels. This is illustrated in Figure 2.

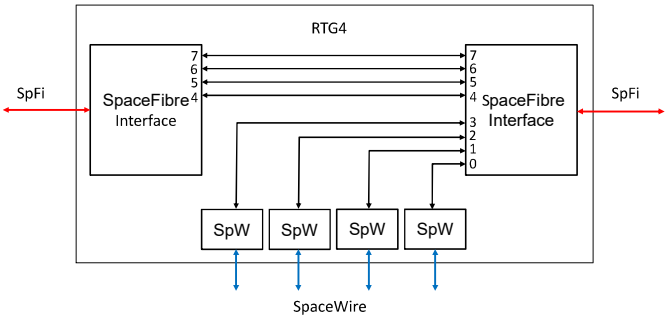


Figure 2. Functional block diagram showing interconnection between SpaceFibre and SpaceWire interfaces in an RTG4 FPGA

The design is implemented on the Microsemi RTG4 development board with SpaceWire and SpaceFibre connectors provided via an FMC board, as shown in Figure 3.

Figure 3. Microsemi RTG4 development board used to test the SpaceFibre interface

The SpaceFibre interfaces operate at up to 3.125 Gbits/s. A multi-lane interface has also been implemented in the RTG4 and validated [10]. The multi-lane IP core has two-lanes with a third lane available in hot or cold standby.

The SUNRISE SpaceFibre routing switch [11] is currently being transferred to the RTG4 FPGA, using a specially designed board [12], which is shown in Figure 4.

Figure 4. Prototype board for SUNRISE SpaceFibre Routers

IV. SpaceFibre Multi-Lane Interface in the RTG4 FPGA

The multi-laning capabilities of the SpaceFibre protocol allow several lanes to operate in parallel to provide enhanced throughput [10]. For example, with four lanes running at 2.5 Gbits/s each an aggregate throughput of 10 Gbits/s is achieved. SpaceFibre multi-laning can operate with any number of lanes, from 1 to 16. Each lane is normally bi-directional, but to support spaceflight instruments with very high-data rate in one direction and to save mass and power, it is possible to have some uni-directional lanes in a multi-lane link, provided that at least one lane is bi-directional. SpaceFibre multi-laning also supports graceful degradation in the event of a lane failure. If a lane fails, the multi-lane link will rapidly reconfigure to use the remaining lanes so that important (high priority) information can still get through. It takes a couple of microseconds for this reconfiguration to occur, which happens without loss of information. Clearly, with reduced bandwidth some information will not be sent over the link, but this will be less important, low priority, information. If a redundant lane is available in the link, it can be enabled and full capacity operation will resume.

Figure 5. Demonstration of SpaceFibre Multi-Laning

The photograph in Figure 5 shows a demonstration of the multi-laning capability of SpaceFibre. A four lane link was demonstrated with low-priority, high-bandwidth traffic flowing over some virtual channels and high-priority video data over another virtual channel. Lanes were unplugged with corresponding loss in bandwidth, but the link continued to operate sending the "critical" video data without interruption. Only when all four lanes were unplugged, did the video data stream cease. As soon as any of the four lanes were plugged back in, the video stream continued once more.

V. SpaceFibre Engineering Model

STAR-Dundee is currently designing a flight Engineering Model level board for the RTG4 which will support SpaceWire and SpaceFibre applications. The architecture of this board is illustrated in Figure 6.

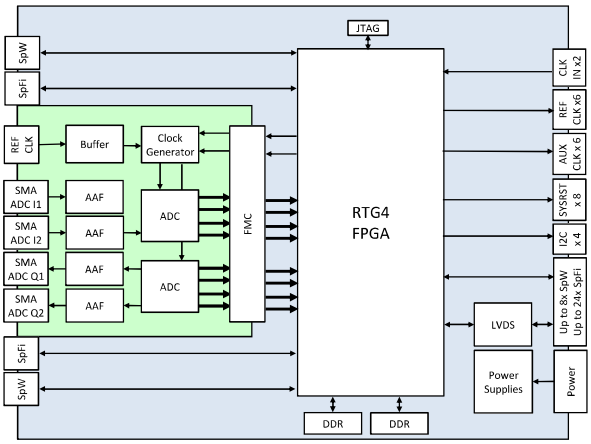


Figure 6. SpaceVPX-RTG4 Board Block Diagram

The SpaceVPX-RTG4 board is a 3U board designed to conform to the emerging VITA78.1 SpaceVPX-Lite standard [13]. The main component on the board is the RTG4 FPGA (PROTO Silicon). It is connected to two independent banks of DDR memory, each supporting Error Detection and Correction (EDAC). Two SpaceWire and two SpaceFibre interfaces are provided on the front panel. The SpaceVPX-Lite backplane supports a SpaceWire control plane and a SpaceFibre data plane along with standard utility plane functions. An FMC type daughterboard connector allows connection to various daughterboards. A dual, 3 Gsamples/s ADC FMC board is available supporting demanding DSP applications. Other daughter boards are planned. The board is conduction cooled.

The board can be configured to operate as a SpaceVPX-Lite System Controller or as a versatile SpaceVPX-Lite Payload Processing board. The System Controller incorporates an ARM Cortex M1 processor running in the FPGA, and has two SpaceWire and two SpaceFibre interfaces on the front panel. It provides the VITA78.1 radial REF_CLK and AUX_CLK signals to each of up to six Payload boards. It can provide either SpaceWire or SpaceFibre radial control plane connections to each Payload board. These control plane interfaces also provide the Payload management function using RMAP [14]. The System Controller is designed to operate in a dual redundant configuration with control plane cross strapping to each Payload board. Cold sparing of the RTG4 is addressed in the board design.

The SpaceVPX-RTG4 board can also act as a Payload board, with control plane connections to each of the two system controller boards. Data plane connections are provided on the board to support full mesh interconnection between the six payload boards.

The components on the board are commercial equivalents of flight grade components.

This board is currently being used to implement the engineering model of a wideband spectrometer for a THz radiometer instrument, being developed in the UK [15]. When fitted with the ADC FMC board each SpaceVPX-RTG4 board will be able to process 1-2 GHz bandwidth signals into 1-5MHz spectral components. The design of the FFT processor is

currently underway based on previous designs implemented and tested in Xilinx Virtex 5 FPGAs.

At present the board is in the PCB layout stage. A physical model of the SpaceVPX-RTG4 board is illustrated in Figure 7.

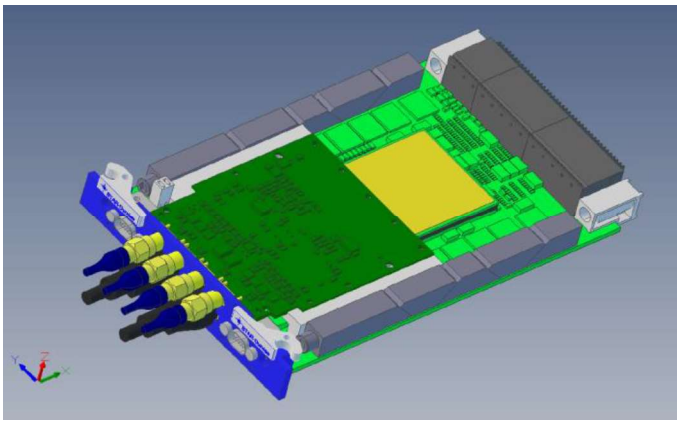


Figure 7. SpaceVPX-RTG4 Physical Model

SpaceVPX-Lite Power Switches and Power Supply modules are also under development along with a backplane and conduction cooled rack.

VI. Ramon Chips RC64

Ramon Chips are developing a many core DSP processing chip in radiation tolerant technology. The RC64 [16], is a novel rad-hard 64-core digital signal processing chip, with a performance of 75 MACS, 150 GOPS and 38 GFLOPS (single precision) and low power consumption, dissipating less than 10 Watts. The RC64 integrates sixty-four advanced DSP cores, a hardware scheduler, 4 MBytes of multi-port shared memory, a DDR2/DDR3 memory interface, and twelve 3.125 Gbps full-duplex, high-speed SpaceFibre serial links, four of which can also support serial Rapid IO.

The RC64 architecture is illustrated in Figure 8. A central scheduler assigns tasks to processors. Each processor executes its task from its cache storage, accessing the on-chip 4MByte shared memory only when needed. When task execution is done, the processor notifies the scheduler, which subsequently assigns a new task to that processor. Access to off-chip streaming channels, DDR2/DDR3 memory, and other interfaces happens only via programmable DMA channels. This approach simplifies software development and it is found to be very useful for DSP applications, which favour streaming over cache-based access to memory. Hardware events, asserted by communication interfaces, initiate software tasks through the scheduler. This enables high event rates to be handled by the many cores efficiently.

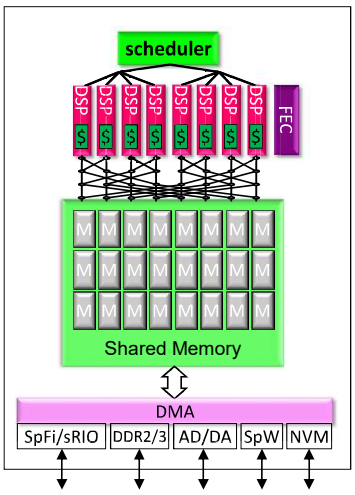


Figure 8. RC64 Many Core DSP Processor Block Diagram (only 8 DSP processors are shown)

The RC64 is implemented as a 300 MHz integrated circuit on a 65nm CMOS technology, assembled in a hermetically sealed ceramic CCGA624 package and qualified to the highest space standards. Supported communication applications include frequency multiplexing, digital beam forming, transparent switching, modems, packet routing and higher-level processing. The 12 SpaceFibre interfaces on the RC64 were designed by STAR-Dundee.

STAR-Dundee is currently designing a SpaceVPX-Lite board containing an RC64 many core DSP processor. A block diagram of this board is shown in Figure 9.

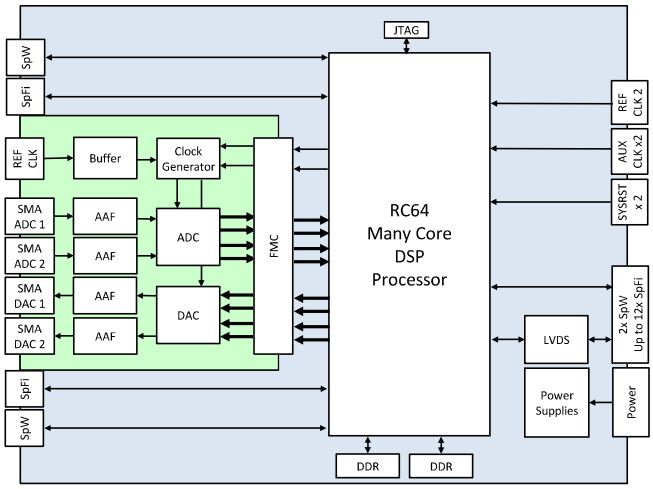


Figure 9. SpaceVPX-RC64 Board Block Diagram

The SpaceVPX-RC64 board contains an RC64 DSP processor attached to DDR memory. The board is designed as a SpaceVPX-Lite Payload board. It receives nominal and redundant REFLCK, AUXCLK and SYSRST signals from the backplane. These signals originate from the nominal and redundant System Controller boards. Nominal and redundant control plane interfaces are also provided from the System

Controller boards via the backplane connectors. The control plane can be either SpaceWire or two-lane SpaceFibre.

There are a pair of SpaceWire interfaces and a pair of SpaceFibre interfaces on the front panel. An FMC connector on the board allows for the connection of a range of FMC type boards to be added. All components on the board are commercial equivalents of radiation tolerant parts. Like the SpaceVPX-RTG4 board the SpaceVPX-RC64 board is conduction cooled.

VII. SpaceFibre Interface Chip

The SpaceFibre ECSS standard is close to being published and SpaceFibre is already being considered for several space missions. There is a need for a range of radiation tolerant SpaceFibre chips to support the missions that plan to use this technology. STAR-Dundee has won a contract from ESA to develop such a device, which is able to meet the instrument interface and avionics equipment requirements for high-speed serial links. This design will build on the extensive experience that STAR-Dundee has with SpaceFibre and in particular on the experimental SpaceFibre interface device designed by STAR-Dundee with European Commission Framework 7 research funding [17].

Conclusions

SpaceFibre is a new generation of the widely used SpaceWire spacecraft on-board data-handling network technology, which has over ten times the performance (per lane) and operates over electrical or fibre optic media. Integrated quality of service and fault detection, isolation and recovery mechanisms enable SpaceFibre to be used for guidance and navigation control, time-distribution, event signalling, command and control, as well as very high data-rate payload data-handling, all with a single, unified network. This reduces cost, mass and risk, improves reliability and simplifies redundancy.

STAR-Dundee has developed a range of SpaceFibre IP cores for spaceflight applications including a single-lane and multi-lane interface targeted for the Microsemi RTG4 and Xilinx Virtex-5QV FPGAs. A SpaceFibre routing switch IP core for the RTG4 is currently under development. STAR-Dundee's IP cores are also being used in a range of radiation tolerant ASIC devices including the Ramon Chips RC64 many core DSP processor and the ESA SpaceFibre Interface Chip. A range of engineering model level boards is being designed by STAR-Dundee based on the emerging VITA 78.1 SpaceVPX-Lite standard. This equipment is targeted at a range of spaceflight signal and image processing applications and is already being designed into the UK LOCUS TeraHertz sounder instrument.

Acknowledgments

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