SpaceFibre: Capabilities, Components and Kit

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ABSTRACT

SpaceFibre is the next generation of SpaceWire network technology for spacecraft on-board data-handling. It runs over electrical or fibre-optic cables, operates at very high data rates, provide in-built quality of service (QoS) and fault detection, isolation and recovery (FDIR) capabilities. This paper introduces SpaceFibre, describes its position as a state-of-the-art network technology for space applications, details it principal capabilities, introduces some of the SpaceFibre components that are available now or will be in the near future, and describes the SpaceFibre test and development equipment available from STAR-Dundee.

1 INTRODUCTION

SpaceFibre [1-5] is a new generation of SpaceWire [5-7] technology which is able to support the very high data-rates required by sensors like SAR and multi-spectral imagers. Data rates of up to 25 Gbps are required to support several sensors currently being planned. In addition, a mass-memory unit requires high performance networking to interconnect many memory modules.

SpaceFibre is designed to support high data-rate payloads, including synthetic aperture radar and hyper-spectral optical instruments. It will provide robust, long distance communications for launcher applications and will support avionics applications with deterministic delivery constraints through the use of virtual channels. SpaceFibre enables a common on-board network to be used across many different mission applications resulting in cost reduction and design reusability.

SpaceFibre runs over both electrical and fibre-optic media and provides 3.125 Gbps data rate in current radiation tolerant FPGA technology and higher data rates of 6.25 Gbps data rate per lane are possible with 65nm technology. SpaceFibre provides a quality of service mechanism which is able to support priority, bandwidth reservation and scheduling. It incorporates fault detection, isolation and recovery (FDIR) capability in the interface hardware. SpaceFibre is designed to be implemented efficiently and has a much smaller footprint than competing technologies such as Serial Rapid IO.

Several SpaceFibre lanes can be operated in parallel (multi-laning) to give higher data rates or increased reliability. A multi-lane link can have any number of lanes from 1 to 16. Multi-lane operation provides hot redundancy and graceful degradation in the event of a lane failure, simplifying redundancy approaches and maintaining essential communication services over the remaining operational lanes. When a lane fault does occur recovery is very fast, taking a few µs. SpaceFibre also supports asymmetric links where some of the lanes can be uni-directional. This is particularly useful for high data-rate instruments where data flow is mainly in one direction, and can save both power and mass.

SpaceFibre is backwards compatible with SpaceWire at the network level, using the same packet format, which allows simple interconnection of existing SpaceWire equipment to a SpaceFibre link or network. SpaceFibre provides many capabilities missing from SpaceWire. Running SpaceWire over a SpaceFibre network can provide those missing capabilities, extending the life of existing SpaceWire equipment designs.

SpaceFibre has a message broadcast capability, which carry eight bytes of user information, together with a broadcast type and channel identifier. This permits, for example, CCSDS unsegmented time information to be broadcast across the spacecraft in a single broadcast message, with low latency. Broadcast messages can be used for time distribution, synchronisation, event signalling, network control and error handling.

2 STATE-OF-THE-ART

SpaceWire is the current de facto standard for spacecraft on-board data-handling networks and is currently being used or designed into more than 100 spacecraft costing well over $30 billion. It has limited performance (up to 400 Mbps), has no quality of service (QoS), has severely limited fault detection, isolation and recovery (FDIR) capability, and does not support data transfer over multiple lanes.

To support data rates above 400 Mbps two main technologies are used at present in spacecraft applications: Channel Link [9] and Wizard Link [10]. Channel link achieve data rates of around 1 Gbps over several parallel

wires. Wizard link achieves a data rate of 2.5 Gbps over a pair of wires in each direction of the link.

Time-Triggered Ethernet (TTE) [11], is an emerging technology for control applications in space. TTE has limited performance (currently 100 Mbps and planned to be 1 Gbps) and requires separate PHY devices or each interface, making the interface large and power hungry. Its use in safety critical applications is well established, but it is not suitable for the spacecraft on-board high-speed data-chain.

Primarily in the USA, there is interest in Serial Rapid Input Output (SRIO) [12] which is a commercial high-speed network for embedded systems. It is being developed by companies like BAE Systems and Honeywell for spacecraft on-board processing applications. BAE Systems are currently developing a range of rad-hard SRIO chips in 45 nm technology which are able to achieve 5 Gbps per lane. Note that commercial SRIO devices can operate at significantly higher speeds. The main issue with SRIO, however, is its high complexity and resultant large footprint.

SpaceFibre is very high-speed data-link and network technology designed specifically for space applications which has a small footprint, taking 3-5% of a current generation radiation tolerant Microsemi RTG4 FPGA allowing plenty of room for the other application specific logic. SpaceFibre is backwards compatible with SpaceWire at the Network level, enabling existing SpaceWire equipment to be connected into a SpaceFibre network without modification. SpaceFibre has been implemented in the Ramon Chips RC64 many core DSP processor and is already being designed into its first space missions even though the ECSS standard is not yet published, showing the driving need for this technology. The ECSS standard is expected to be published in 2017.

3 SPACEFIBRE CAPABILITIES

SpaceFibre has been designed specifically to support space flight applications. Its main characteristics and capabilities are listed below:

- **Very high-performance** with 3.125 Gbps single-lane performance in current radiation tolerant FPGAs, 12.5 Gbps with four lanes, and substantially high data rates planned in future devices.
- **Electrical and Fibre Optic media** with the electrical medium supporting cable lengths up to 5 m and fibre optics supporting up to 100 m.
- **High reliability and high availability** using error-handling technology which is able to recover automatically from transient errors in a few µs without loss of information and which is able to continue operation preserving data transfer of critical and important information when a lane in a multi-lane link fails.
- **Quality of service** using multiple virtual channels across a data link, each of which is provided with a priority level, a bandwidth allocation and a schedule.
- **Virtual networks** that provide multiple independent traffic flows on a single physical network, which when mapped to a virtual channel acquires the quality of service of that virtual channel.
- **Deterministic data delivery** of information using the scheduled quality of service, in conjunction with priority and bandwidth allocation.
- **Low latency broadcast messages** which provide time-distribution, synchronisation, event signalling, error reporting and network control capabilities.
- **Small footprint** which enables a complete SpaceFibre interface to be implemented in a radiation tolerant FPGA e.g. around 3% of an RTG4 FPGA for an interface with two virtual channels.

4 SPACEFIBRE COMPONENTS

4.1 SpaceFibre IP Cores

STAR has developed a comprehensive set of IP cores for SpaceFibre which are already being used in their first space missions and ASIC designs. Both single-lane and multi-lane IP cores are available from STAR. In addition STAR has a prototype SpaceFibre router design which is currently being ported to radiation tolerant FPGAs. The follow IP cores are now available from STAR-Dundee targeted for Microsemi RTG4 and Xilinx FPGAs, and ASIC implementation:

- Single-lane interface;
- Multi-lane interface;
- SpaceWire to SpaceFibre bridge;
- Routing switch.

Figure 1 shows STAR SpaceFibre routers, SpaceFibre to SpaceWire bridges and SpaceFibre interfaces being demonstrated.

Figure 1: SpaceFibre Network Demonstration

4.2 RC64 Many Core DSP Processor

Ramon Chips are developing a many core DSP processing chip in radiation tolerant technology. The RC64, is a novel rad-hard 64-core digital signal processing chip, with a performance of 75 MACS, 150 GOPS and 38 GFLOPS (single precision) and low power consumption, dissipating less than 10 Watts. The RC64 integrates sixty-four advanced DSP cores, a hardware scheduler, 4 MBytes of multi-port shared memory, a DDR2/DDR3 memory interface, and twelve 3.125 Gbps full-duplex, high-speed

SpaceFibre serial links, four of which can also support serial Rapid IO.

The RC64 architecture is illustrated in Figure 2. A central scheduler assigns tasks to processors. Each processor executes its task from its cache storage, accessing the on-chip 4MByte shared memory only when needed. When task execution is done, the processor notifies the scheduler, which subsequently assigns a new task to that processor. Access to off-chip streaming channels, DDR2/DDR3 memory, and other interfaces happens only via programmable DMA channels. This approach simplifies software development and it is found to be very useful for DSP applications, which favour streaming over cache-based access to memory. Hardware events, asserted by communication interfaces, initiate software tasks through the scheduler. This enables high event rates to be handled by the many cores efficiently.

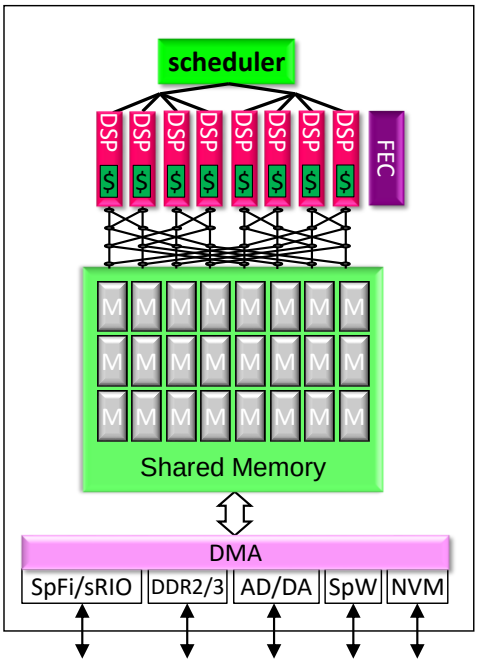

Figure 2: RC64 Many Core DSP Processor Block Diagram (only 8 DSP processors are shown)

The RC64 is implemented as a 300 MHz integrated circuit on a 65nm CMOS technology, assembled in a hermetically sealed ceramic CCGA624 package and qualified to the highest space standards. The 12 SpaceFibre interfaces on the RC64 were designed by STAR-Dundee.

5 SPACEFIBRE KIT

5.1 STAR Fire Mk3

The STAR Fire Mk3 is the evolution of the initial STAR Fire device. It has two SpaceFibre and two SpaceWire interfaces, two Mictor connectors for connecting a Logic Analyser, and four SMB connectors. Three of those are external input triggers, and one is an external output trigger. Figure 3 shows the block diagram of the STAR Fire Mk3 design and Figure 4 is a photograph.

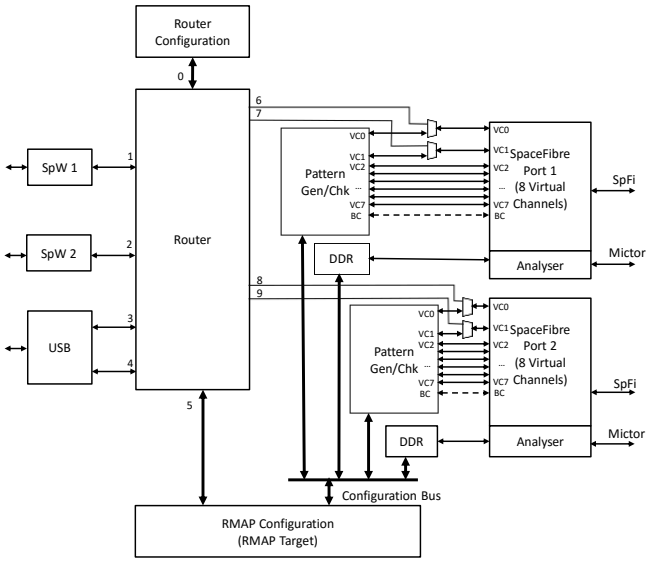

Figure 3: *STAR Fire Mk3 architecture*

The STAR Fire Mk3 can operate as a SpaceFibre link analyser, SpaceFibre interface and as a bridge between SpaceFibre and SpaceWire. It has embedded pattern data generators and checkers for high data-rate packet generation and checking. The Mk3 has a USB 3.0 interface, which provides high data-rate communications with a host PC.

Figure 4: *STAR Fire Mk3 unit*

5.2 SpaceFibre Link Analysis Software

The STAR Fire is able to operate as a SpaceFibre Link Analyser. The STAR Fire unit can transparently capture SpaceFibre traffic on a single link in both directions. The point around which traffic is captured is known as a trigger. The STAR Fire can trigger upon detection of SpaceFibre words, symbol patterns or errors.

To display the captured SpaceFibre traffic, three independent views are provided. When a SpaceFibre traffic item is selected in one view, each of the other views automatically navigate to their corresponding item.

5.3 Symbol View

The Symbol View displays the traffic captured in both directions of a SpaceFibre link as symbols and words. The view is divided into two sides: the left side displays the traffic flowing in one direction, and the right side displays the traffic flowing in the opposite direction. In the left-most column, the word index is shown, which is relative to the trigger point. Figure 5 shows a screenshot of the

Symbol View displaying traffic flowing in both directions on a SpaceFibre link.

Symbol View

	Symbol 1	Symbol 2	Symbol 3	Symbol 4	End A Word	End B Word	Symbol 1	Symbol 2	Symbol 3	Symbol 4
0	Comma	SDF	0x02	0x00	SDF (VC 2)	DATA (5)	0x05	0x00	0x00	0x00
1	0x0e	0x00	0x00	0x00	DATA (14)	DATA (6)	0x06	0x00	0x00	0x00
2	0x0f	0x00	0x00	0x00	DATA (15)	DATA (7)	0x07	0x00	0x00	0x00
3	Comma	ACK	0x02	0xde	ACK (SEQ ...	DATA (8)	0x08	0x00	0x00	0x00
4	EOP	Fill	Fill	Fill	DATA (EOP)	DATA (9)	0x09	0x00	0x00	0x00
5	0x00	0x00	0x00	0x00	DATA (0)	DATA (10)	0x0a	0x00	0x00	0x00
6	0x01	0x00	0x00	0x00	DATA (1)	DATA (11)	0x0b	0x00	0x00	0x00
7	0x02	0x00	0x00	0x00	DATA (2)	ACK (SEQ ...	Comma	ACK	0x4c	0x44
8	0x03	0x00	0x00	0x00	DATA (3)	DATA (12)	0x0c	0x00	0x00	0x00
9	0x04	0x00	0x00	0x00	DATA (4)	DATA (13)	0x0d	0x00	0x00	0x00
10	0x05	0x00	0x00	0x00	DATA (5)	DATA (14)	0x0e	0x00	0x00	0x00
11	0x06	0x00	0x00	0x00	DATA (6)	DATA (15)	0x0f	0x00	0x00	0x00
12	0x07	0x00	0x00	0x00	DATA (7)	DATA (EOP)	EOP	Fill	Fill	Fill
13	0x08	0x00	0x00	0x00	DATA (8)	DATA (0)	0x00	0x00	0x00	0x00
14	0x09	0x00	0x00	0x00	DATA (9)	DATA (1)	0x01	0x00	0x00	0x00
15	0x0a	0x00	0x00	0x00	DATA (10)	DATA (2)	0x02	0x00	0x00	0x00
16	0x0b	0x00	0x00	0x00	DATA (11)	DATA (3)	0x03	0x00	0x00	0x00
17	0x0c	0x00	0x00	0x00	DATA (12)	DATA (4)	0x04	0x00	0x00	0x00
18	0x0d	0x00	0x00	0x00	DATA (13)	DATA (5)	0x05	0x00	0x00	0x00
19	0x0e	0x00	0x00	0x00	DATA (14)	DATA (6)	0x06	0x00	0x00	0x00
20	0x0f	0x00	0x00	0x00	DATA (15)	DATA (7)	0x07	0x00	0x00	0x00

Figure 5: Symbol View

In Figure 5, the trigger point is shown as a yellow row in the table. In this case, the STAR Fire was configured to trigger when a Start of Data Frame (SDF) word was detected on End A of the link.

5.4 Frame View

The Frame View displays captured traffic as data and broadcast frames. Each frame is shown within a column representing the channel with which it is associated. The Frame View is divided into two sides, one for each link direction. In each direction, broadcasts are displayed in a broadcasts column and frames are displayed in virtual channel (VC) columns. In Figure 6, a broadcast column and four VC columns are displayed showing the broadcast and data frames captured in both directions. The captured traffic is the same as the Symbol View example.

Frame View

	BC	VC 0	VC 1	VC 2	VC 3	BC	VC 0	VC 1	VC 2	VC 3
0				SDF (64 ...						
4				EOP						
12									EOP	
21				EOP						
29									EOP	
38				EOP						
47									EOP	
57				EOP					EDF (Se...	
58							SDF (64...			
69				EDF (Se...						
70				SDF (64 ...						
77				EOP						
94				EOP						
113				EOP						
126	SBF(BC 1...						EDF (Se...			
127	BF FILLER					SBF(BC...				
129	EBF (Seq...					BF FILL...				
130						EBF (Se...				
131								SDF (64...		
135				EOP						
142				EDF (Se...				EOP		

Figure 6: Frame View

In Figure 6, the SDF that triggered the traffic capture is shown in the first row. The data frame is displayed in the column for virtual channel 2 on End A. In this example, additional data frames are shown in VC2 on End A and VC0, VC1 and VC2 on End B. A broadcast frame for each end is displayed in the BC columns.

5.5 Network View

The Network View displays large amounts of captured traffic as activity on a horizontal timeline. The captured traffic can be navigated by panning, zooming or selecting areas of interest. The view is divided into rows representing virtual networks or broadcast messages.

Figure 7 shows an example of the Network View displaying the same captured traffic as the Symbol and Frame Views.

In

Figure 7, the four virtual channels are shown in the first four rows and the broadcast messages are shown in the fifth row. Each row is divided into a top and bottom half representing Ends A and B of the link, respectively. Data frames are shown as blue bars with EOPs indicated as vertical lines within the frames. At the top of the view there is a timeline showing a preview of the entire traffic capture, with a green bar showing the currently visible region.

5.6SpaceFibre PXI Board

The SpaceFibre PXI board has been developed to implement a range of SpaceWire and SpaceFibre devices. The board is a 3U compatible with PXI, Compact PCI (cPCI) or PXIe racks.

The board offers DDR memory and programmable clock sources to provide the end user with a very flexible architecture to implement multiple designs. It features a novel set of front panel interconnects. There is a set of flexible interface connectors that can be used to customise the board, such as SpaceFibre, SpaceWire, external triggers, etc. Thus, the board can be easily modified to accommodate different designs. This allows using the same PXI board to implement many different products.

Several designs have already been implemented using the PXI Board, such as the SUNRISE 8-port SpFi Router (Figure 8), a 4-port SpaceFibre interface, a Multilane (up to 4 lanes) SpaceFibre interface and a SpaceWire to SpaceFibre bridge.

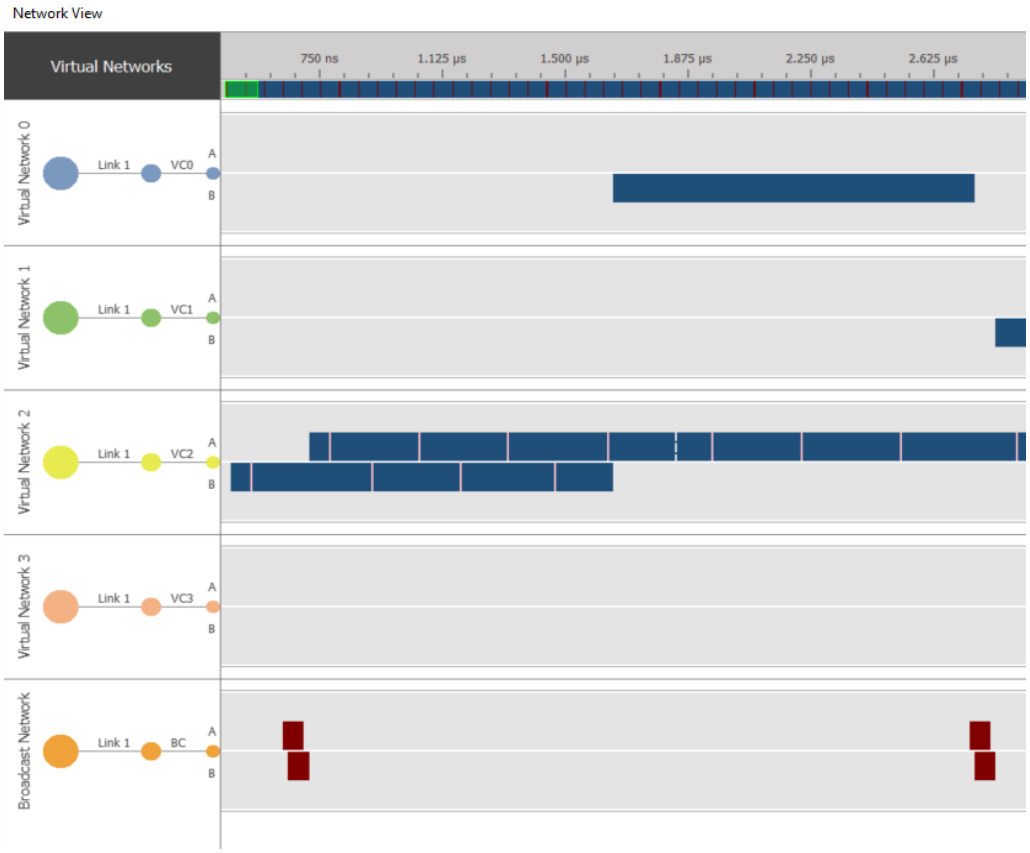

Figure 7: Network View

Figure 8. PXI Board configured as SpaceFibre Router

5.7 PXIe-RTG4

The PXIe-RTG4 board is a versatile development board for the Microsemi RTG4 FPGA. The Microsemi RTG4 is a new generation radiation tolerant FPGA. It has extensive logic, memory, DSP blocks, and IO capabilities and is inherently radiation tolerant, having triple mode redundancy built in. The RTG4 has a flash configuration memory built into the device. In addition the FPGA incorporates 16 SpaceWire clock-data recovery circuits and 24 multi-Gbits/s SerDes lanes to support high-speed serial protocols like SpaceFibre.

On the PXIe-RTG4 board there are two banks of 32-bit wide DDR memory attached to the RTG4, each with EDAC parity protection. The board is a 3U PXIe board with 5 Volt power taken from backplane connector. A four lane PCIe interface is provided on the backplane along with PXI triggers. Programmable clock generators are also provided on the board.

A set of STAR-Dundee “flexi” connectors are provided for attaching SpaceWire, CAN bus, UART and other IO functions to the board. In addition there are two, four lane SpaceFibre interfaces using the SerDes integrated into the RTG4 FPGA. These SpaceFibre interfaces can be used to provide eight, single-lane SpaceFibre interfaces or two, four-lane interfaces, or other combinations.

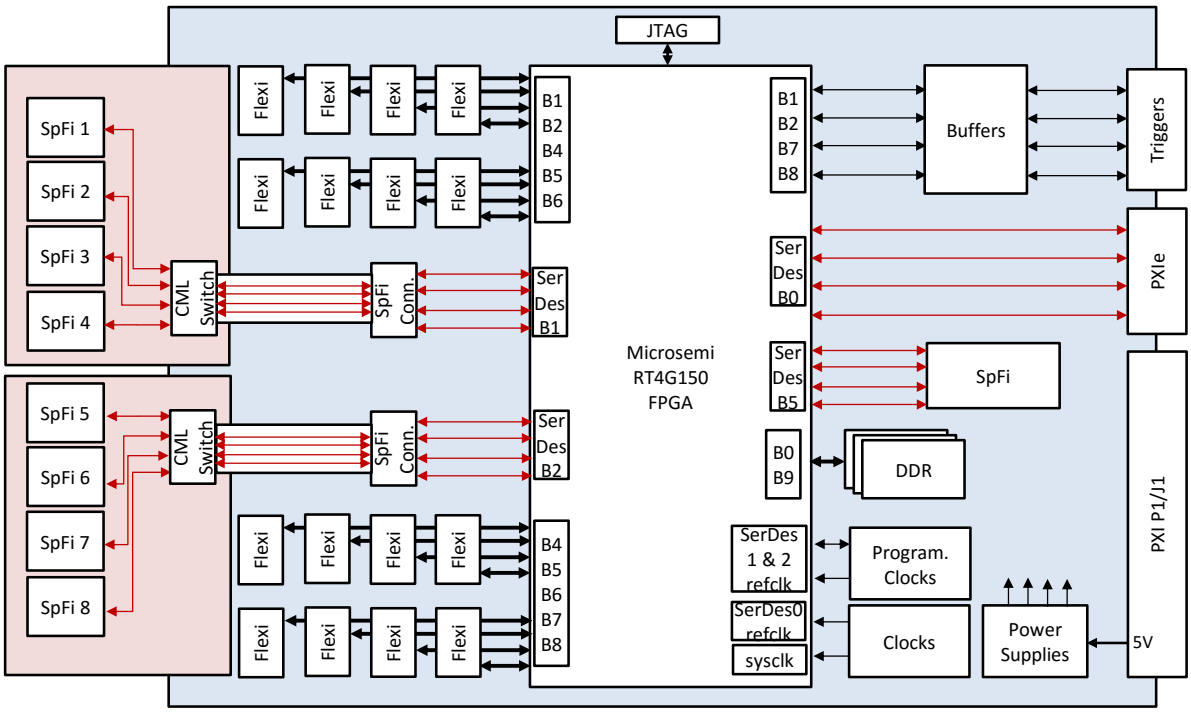

Figure 9: PXIe-RTG4 Board

5.8SpaceVPX-RTG4

The SpaceVPX-RTG4 board is a 3U conduction cooled board containing an RTG4 FPGA. A block diagram of this board is shown in Figure 10 along with a CAD model in Figure 11

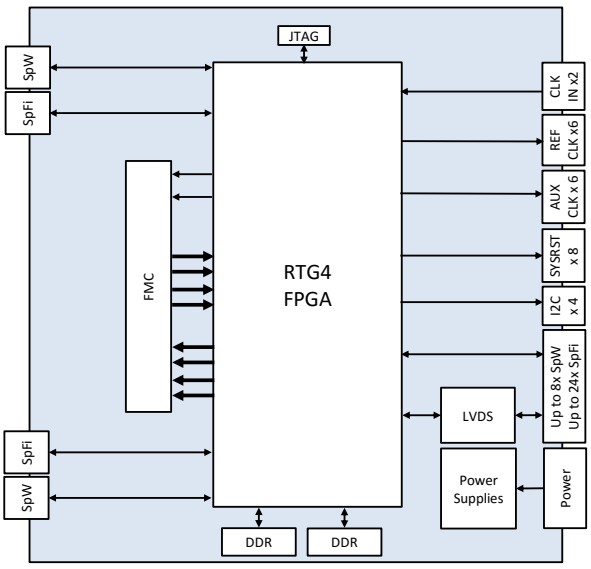

Figure 10: SpaceVPX-RTG4 Board Block Diagram

The RTG4 can be configured as either a SpaceVPXLite (VITA 78.1) system controller or a payload processor. It provides the following sets of signals to the SpaceVPXLite backplane:

- Power connections from the power switch module.
- Control plane comprising either six SpaceWire links or six, four-lane SpaceFibre links.
- I2C buses to the two power supplies and power switch, used for control and status monitoring of these boards.
- Eight system reset signals, which fan out radially to the six payload processors and to the power supply and switch board.
- Six reference clocks, which are sent radially to the payload processors.
- Six auxiliary clock (synchronisation or periodic pulse signals), which are also sent radially to the payload processors.
- A pair of clock inputs, which are used to derive the clock output signals when the board is acting as a system controller and which provide the nominal and redundant clock inputs when operating as a payload module.

Attached to the RTG4 are two banks of 32-bit wide DDR memory each with 8-bit EDAC parity. A pair of SpaceWire and a pair of SpaceFibre connectors are provided on the front panel of the SpaceVPX-RTG4 board. To provide additional input/output functions an FMC connector is provided on the board. Several FMC boards are being designed to operate with the SpaceVPX-RTG4 board including a 2.4 Gsamples/s, dual ADC board.

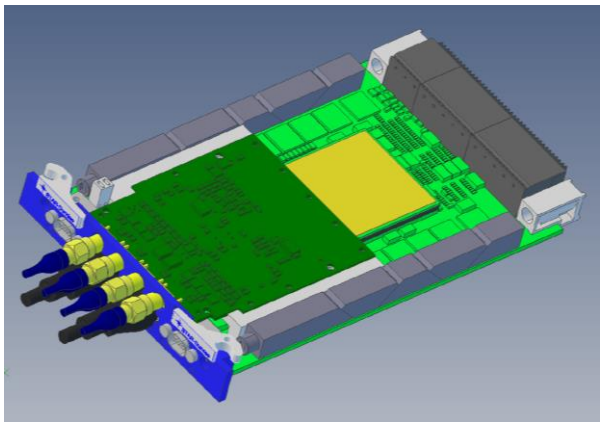

Figure 11: SpaceVPX-RTG4 Board CAD Model with FMC Card Fitted

6 CONCLUSIONS

SpaceFibre provides multi-gigabit/s communications. It incorporates a comprehensive quality of service capability providing integrated bandwidth reservation, priority and scheduling. Efficient, effective and rapid fault detection, isolation and recovery mechanisms are included in the SpaceFibre interface, enabling rapid detection and recovery from link level errors. SpaceFibre multi-laning allows the very high data rates to be achieved which are necessary for future SAR and multi-spectral imaging instruments. SpaceFibre routing switches allow the construction of complete SpaceFibre physical networks carrying several independent virtual networks. STAR-Dundee can provide the necessary chip designs and test and development equipment to implement SpaceFibre. The SpaceFibre standard is due for publication as an ECSS standard in mid-2017.

7 ACKNOWLEDGMENTS

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