SpaceFibre Camera

On-board Equipment and Software, Long Paper

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***Abstract*—SpaceFibre is a high performance, high availability technology for space flight and other demanding applications. The recent generation of image sensors are capable of data rates of several Gbps. SpaceFibre is ideal as an interface to such an image sensor. STAR-Dundee has designed a complete camera, which incorporates a radiation tolerant FPGA for sensor interfacing and control, and image signal processing. This paper introduces SpaceFibre, the Microsemi RTG4 FPGA, the CMV4000 image sensor and describes the complete SpaceFibre camera.**

***Index Terms*—SpaceFibre, Image Sensor, SpaceWire, Networking, Spacecraft Electronics, Radiation Tolerant, FPGA, RTG4.**

I. Introduction

SpaceFibre [1-4] is a new generation of SpaceWire [5-6] technology which is able to support the very high data-rates required by sensors like SAR and multi-spectral imagers. Data rates of up to 25 Gbps are required to support several sensors currently being planned. In addition, a mass-memory unit requires high performance networking to interconnect many memory modules.

To support the development of spaceflight equipment incorporating SpaceFibre, STAR-Dundee has developed a range of SpaceFibre IP cores and SpaceFibre test and development equipment. The IP cores are being used in radiation tolerant FPGA and ASICs. Recently STAR-Dundee has designed a SpaceFibre camera and a SpaceVPX based processing board to demonstrate the ease with which SpaceFibre can be integrated into spaceflight systems and the substantial advantages it can bring.

This paper first introduces SpaceFibre. It then describes the main components of the SpaceFibre camera; the Microsemi RTG4 radiation tolerant FPGA and the CMOSIS CMV4000 image sensor. The SpaceFibre camera is then described in detail.

II. SpaceFibre

SpaceFibre is designed to support high data-rate payloads, including synthetic aperture radar and hyper-spectral optical instruments. It provides robust, long distance communications for launcher applications and supports avionics applications with deterministic delivery constraints through the use of virtual channels. SpaceFibre enables a common on-board network to be used across many different mission applications resulting in cost reduction and design reusability.

SpaceFibre runs over both electrical and fibre-optic media and provides 3.125 Gbps data rate in current radiation tolerant FPGA technology. Higher data rates of 6.25 Gbps data rate per lane are possible with 65nm ASIC technology. SpaceFibre provides a quality of service mechanism which is able to support priority, bandwidth reservation and scheduling. It incorporates fault detection, isolation and recovery (FDIR) capability in the interface hardware. SpaceFibre is designed to be implemented efficiently and has a much smaller footprint than competing technologies such as Serial Rapid IO, taking 3-5% of a Microsemi radiation tolerant RTG4 FPGA [7-8] which allows plenty of room for the application specific logic.

Several SpaceFibre lanes can be operated in parallel (multi-laning) to give higher data rates or increased reliability. A multi-lane link can have any number of lanes from 1 to 16. Multi-lane operation provides hot redundancy and graceful degradation in the event of a lane failure, simplifying redundancy approaches and maintaining essential communication services over the remaining operational lanes. When a lane fault does occur, recovery is very fast, taking a few µs. SpaceFibre also supports asymmetric links where some of the lanes can be unidirectional. This is particularly useful for high data-rate instruments where data flow is mainly in one direction, and can save both power and mass.

SpaceFibre is backwards compatible with SpaceWire at the network level, using the same packet format, which allows simple interconnection of existing SpaceWire equipment to a SpaceFibre link or network.

SpaceFibre has a message broadcast capability, which carries eight bytes of user information, together with a broadcast type and channel identifier. This permits, for example, CCSDS unsegmented time information to be broadcast across the spacecraft in a single broadcast message, with low latency. Broadcast messages can be used for time distribution, synchronisation, event signalling, network control and error handling.

The ECSS-E-ST-50-11C SpaceFibre standard will be published in November 2018.

STAR-Dundee has developed a comprehensive set of IP cores for SpaceFibre which are already being used in their first space missions and ASIC designs. Both single-lane and multi-lane IP cores are available. In addition, STAR-Dundee has a SpaceFibre router design running on radiation tolerant FPGAs. The following IP cores are now available from STAR-Dundee targeted for Microsemi RTG4 and Xilinx FPGAs, and ASIC implementation:

- Single-lane SpaceFibre interface;
- Multi-lane SpaceFibre interface;
- SpaceWire to SpaceFibre bridge;
- SpaceFibre routing switch.

III. Microsemi RTG4 FPGA

The RTG4 FPGA is a radiation tolerant FPGA from Microsemi which is fully reprogrammable and which has an integrated flash memory to store configuration information. The RTG4 architecture is illustrated in Fig. 1.

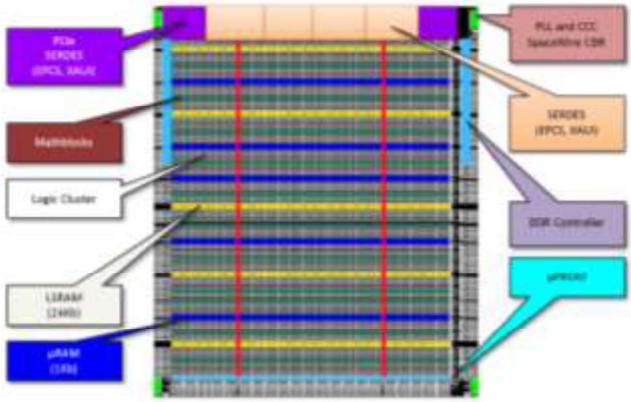

Fig. 1. Microsemi RTG4 FPGA Architecture

The RTG4 contains 151,824 logic elements each comprising a 4-input LUT and flip-flop capable of operating at a clock speed of 250 MHz. There are 209 blocks of dual-port SRAM which can each be configured as 512 x 36, 1 kbit x 18, 2 kbit x 9 or 2 kbit x 12 memory blocks. The RTG4 also includes 210 three-port SRAM blocks which can each be configured as 64 x 18, 128 x 12 or 128 x 9. To access external memory there are two high-speed DDR2/DDR3 memory controllers which can operate at 333MHz and support x9, x12, x18 and x36 bus widths. The memory controllers provide optional error detection and correction (EDAC) for the external memory devices.

The RTG4 has 462 math blocks, each of which contains an 18x18-bit multiplier and a 44-bit accumulator. The math blocks can provide 250 MHz pipelined performance giving a total potential DSP performance of 230 GOPS. The math blocks are ideal for many DSP functions including filters and Fast Fourier Transforms (FFTs). A FFT spectrometer, implemented by STAR-Dundee in the RTG4 FPGA, achieved a DSP performance of 100 GOPS [9].

To implement SpaceFibre a high-speed serialiser/de-serialiser (SerDes) is required, which takes relatively slow, parallel data and serialises it for transmission at high-speed and de-serialises the received serial data to recover the parallel data stream. The RTG4 FPGA includes 24 high-speed (3.125 Gbps) SerDes on-chip avoiding the need for external SerDes devices. These integrated SerDes make the RTG4 ideal for the implementation of spaceflight data-handling and processing sub-systems with multi-Gbps SpaceFibre interfaces. STAR-Dundee has a range of SpaceFibre IP cores which are optimized for the RTG4. The RTG4 has 16 SpaceWire clock and data recovery circuits, which support SpaceWire interfaces running at up to 180 Mbps.

The 65nm flash process used in the RTG4 devices is intrinsically immune to configuration upsets, and the devices also feature additional radiation protection for data in flip-flops and combinatorial logic elements, embedded SRAM cells and multiply accumulate blocks. The RTG4 is designed to eliminate single-event latch-ups.

IV. Image Sensor

An image sensor was required for the SpaceFibre camera which had reasonable resolution, was capable of generating data at data rates in excess of 5 Gbps and had flight heritage. The CMV4000 from CMOSIS was selected.

The main characteristics of the CMV4000 are listed below:

- Monochrome 2k x 2k pixels;
- Colour version available with 1k x 1k pixels;
- Global shutter;
- Exposure during readout;
- Correlated double sampling;
- Integrated ADCs;
- Selectable resolution of 10-bits or 12-bits;
- Multiple high dynamic range options;
- 16, 8, 4 or 2 channel LVDS outputs;
- On-chip programmable PLL for high-speed clock generation;
- Maximum frame rate of 180 frames per second;
- Successfully flown in space missions.

These characteristics make the CMV4000 ideal, in many ways, for the SpaceFibre camera. A maximum data rate well above the capability of a single-lane SpaceFibre interface is readily achieved, permitting experimentation with multi-lane interfaces to the camera.

V. SpaceFibre Camera

The SpaceFibre camera provides a high-resolution, high frame-rate camera which is suitable for both Earth Observation, vision-based navigation and robotic applications. It incorporates the Microsemi RTG4 FPGA which, as well as providing the image sensor interface, control logic and SpaceFibre interfaces, has plenty of room left for data compression or other image processing applications to be integrated in the camera. One specific example, of interest to the team at Dundee, is image feature extraction and tracking for vision-based navigation of planetary landers.

A block diagram of the SpaceFibre Camera is provided in Fig. 2.

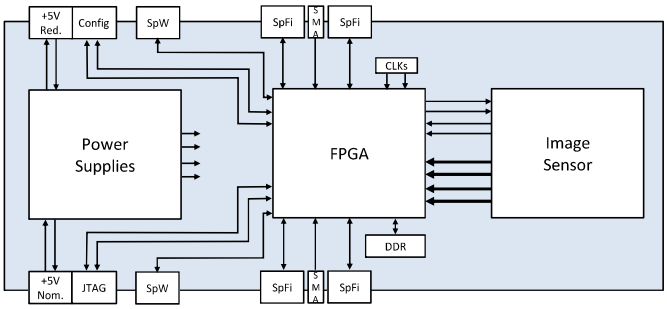

Fig. 2. SpaceFibre Camera Block Diagram

There are ten connectors on the SpaceFibre camera: four SpaceFibre connectors (2-lane nominal and 2-lane redundant), two SMA trigger input connectors, two SpaceWire connectors (nominal and redundant) and +5V DC power connectors (nominal plus JTAG and redundant plus configuration).

The CMV4000 image sensor is configured and controlled by the RTG4 FPGA. The image sensor sends image data to the FPGA via 16 LVDS differential pairs running at up to 480 Mbps per pair. The FPGA includes four SpaceFibre lanes which can operate as two 2-lane links or one 4-lane link. When operating with two 2-lane links, one is active and the other is redundant. The FPGA transfers the image data out of the camera over the active SpaceFibre link. There are also two SpaceWire interfaces (nominal and redundant) which can be used for transferring data instead of using the SpaceFibre interfaces.

Camera configuration, control and housekeeping requests are received over virtual channel 0 of the active SpaceFibre link or over the active SpaceWire link when in SpaceWire interface mode. The FPGA interprets these commands and transfers information to and from the image sensor accordingly, using the control interface of the image sensor.

Attached to the image sensor is a bank of EDAC protected DDR memory which can be used to store images when the FPGA is being used as an image processor.

Power is provided to the SpaceFibre camera via a pair (nominal and redundant) of 15-pin micro-D connectors. The input power is DC-DC converted to the various power supplies required by the FPGA and image sensor. Power on reset circuitry is also provided to reset the FPGA and image sensor during power-up.

The JTAG interface for programming and debugging the FPGA is accessible using the spare pins of the nominal power connector. Six system configuration signals are similarly set using the spare pins of the redundant power connector. These six pins may also be used for debug input/output. The two SMA connectors provide two trigger inputs which are buffered using Schmitt triggers and passed to the FPGA.

A crystal oscillator is provided for the FPGA for general operation along with a programmable oscillator for the SpaceFibre links. A flexi connector is connected to spare pins of the FPGA for test and debug use.

The SpaceFibre camera electronics is implemented on a single flexi-rigid PCB as illustrated in Fig. 3. The blue areas represent the rigid part of the PCB and the green the flexible part. The power supply circuitry is on one board, along with the SpaceWire connectors, and power supply/configuration connectors. The RTG4 is on the middle board, together with the DDR memory and the four SpaceFibre connectors, to minimise the PCB track lengths from the FPGA. The image sensor is on the third board, along with the power supplies for the image sensor. The LVDS lines from the image sensor run through the flexi part of the PCB to the FPGA.

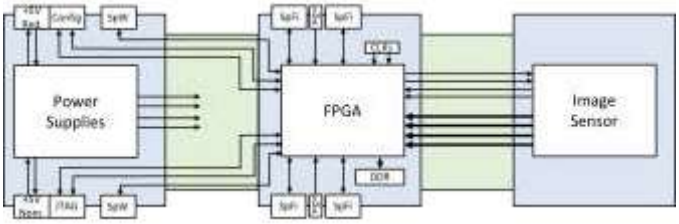

Fig. 3. Arrangement of SpaceFibre Camera Functions on Flexi-Rigid PCB

A photograph of the flexi-rigid PCB or the SpaceFibre Camera is illustrated in Fig. 4.

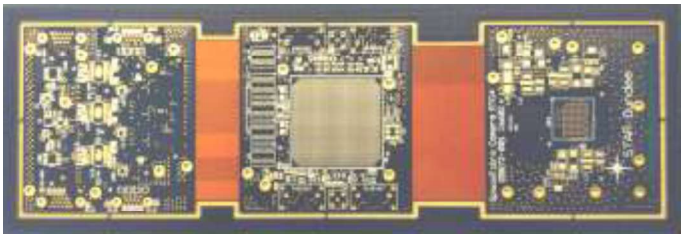

Fig. 4. Flexi-Rigid PCB for SpaceFibre Camera

The pad grid for the FPGA can be clearly seen. The size of the FPGA 42.5x 42.5 mm was the main driver for the size of the camera. The PCB is folded with the FPGA facing down, the power board folded over the rear of the FPGA board and the image sensor board folded over the power supply board. This results in the image sensor being visible at the front of the camera and the FPGA being lid down at the rear. A thermal plastic layer conducts heat directly from the lid of the FPGA to the base on the rear of the camera.

The populated PCB can be seen in Fig. 5. There is a socket for the image sensor so that a monochrome or colour version can be fitted.

The housing for the camera was designed so that the PCB could be mounted on separate parts of the housing. The housing with the PCB is then folded up and held in position with some bolts. A CAD model of the camera was constructed, see Fig. 6. , and this was then implemented as a 3D printed plastic housing to check the mechanical arrangement. The various mechanical parts were then machined in aluminium and the complete camera constructed. A C-mount was used to fit the lens to the camera housing. It is possible to shim the lens to provide the correct back focal length. The complete camera is shown in Fig. 7. and a partially assembled camera is shown in Fig. 8.

Fig. 5. Assembled SpaceFibre Camera PCB

Fig. 6. SpaceFibre Camera CAD Model

Fig. 7. SpaceFibre Camera Housing

Fig. 8. SpaceFibre Camera Partly Installed in Box

An initial test design was developed for the RTG4 FPGA which was used to check the correct operation of most of the elements of the SpaceFibre camera. A block diagram of this FPGA design is shown in Fig. 9. The image sensor interface is on the right-hand side of this diagram. A 100 MHz oscillator on the PCB provides the basic clock signal to the FPGA. This is fed through a global clock generator to provide the clocks required inside the FPGA. The bit and word clocks required by the image sensor are produced by a clock generator circuit and passed to the image sensor using LVDS signals. The image data from the image sensor is passed back on 16 LVDS signal pairs together with a control signal which indicates when the data on the data lines is valid and a clock which is synchronous with the data. The data is clocked into the FPGA by a camera readout circuit. The data is passed as sixteen12-bit data streams into a packet encapsulator. Each image frame is encapsulated in a separate packet. Header information is added to the start of packet and it is terminated by an end of packet market (EOP). The packet data is then passed to virtual channel VC1 of SpaceFibre interface SpFi1. It is passed through the SpaceFibre interface and Serialiser/Deserialiser (SerDes0) and out of the FPGA pins to one of the SpaceFibre connectors on the PCB. At present the image data is only connected to SpFi1, but in future it will also be connected to virtual channel VC1 of SpFi2, which will act as a redundant SpaceFibre interface or part of a dual-lane or quad-lane interface.

Virtual channel VC0 of the two SpaceFibre interfaces are connected to an internal SpaceWire router, which also connects to the two SpaceWire interfaces on the camera. The SpaceWire router connects to a configuration port (port 0 on the router) which is used to access the configuration, control and monitoring interfaces of the SpaceFibre interfaces, SpaceWire interface and the SpaceWire routing switch. Configuration is done using Remote Memory Access Protocol (RMAP) commands. Port 5 of the SpaceWire routing switch is connected to a second RMAP interface which is used to talk to the image sensor control interface. The image sensor is configured and controlled via an SPI interface. RMAP commands arriving over SpaceFibre or SpaceWire are converted into SPI commands which read and write registers inside the image sensor chip. The Frame Request control signals are also configured and controlled via the RMAP interface.

There is a DDR memory interface on the FPGA, but this has not yet been tested. It will be used for storing image data when performing image processing tasks in the RTG4 FPGA.

After initial testing and debugging the SpaceFibre camera was brought into operation. An image display application on a PC was able to capture and display the image data at a frame rate of around 19 Hz. For simplicity, each image pixel was packed into a sixteen-bit word. The resulting data rate is around 1.2 Gbps. The camera is capable of much higher frame rates and with a single SpaceFibre link it is expected that a frame rate of 20 Hz should be possible.

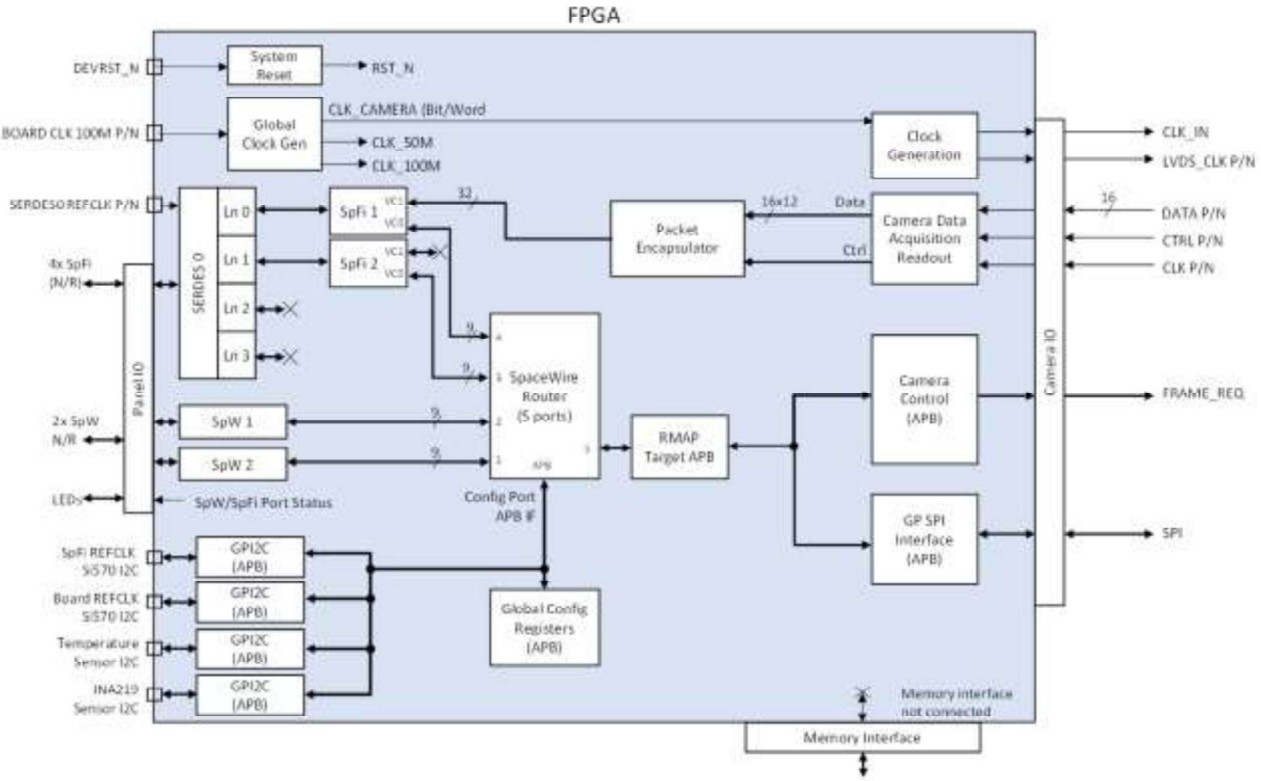

Fig. 9. SpaceFibre Camera Initial FPGA Design

VI. Conclusions and Future Work

The SpaceFibre camera is operational and running well with a single SpaceFibre link. An image display application on a host PC is able to receive and display data at a frame rate of around 19 Hz, corresponding to a data rate of 1.2 Gbps. The data rate can be increased by simply changing some registers in the image sensor. The complete camera interfaces, SpaceFibre interfaces, SpaceWire interfaces, SpaceWire router and configuration logic take around 10% of the RTG4 FPGA leaving plenty of FPGA resources for the image processing applications.

Now that the image acquisition has been shown to be working, the next step in the project is to complete a more comprehensive FPGA design, which will permit redundant single-lane, redundant dual-lane and quad lane operation of the SpaceFibre interfaces. It will also incorporate the DDR memory and provide some example image processing applications on the RTG4.

As well as using the SpaceFibre interfaces for sending data from an image sensor to a mass-memory unit, it is possible to pass data between image sensors, since there are four SpaceFibre interfaces in each camera. The use of this capability for stereo-vision processing distributed between two cameras will be explored.

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