

SpaceVPX-RTG4 Board with SpaceWire or SpaceFibre Backplane

On-board Equipment and Software, Long Paper

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Abstract— SpaceVPX (VITA 78.0) is built on the ruggedized VPX standard. It addresses the need for redundancy in spaceflight systems and focusses on conduction cooled racks. SpaceVPX replaces the VMEbus control-plane of VPX with SpaceWire, while retaining the versatility of a user defined data plane serial interconnect. SpaceVPX-Lite (VITA 78.1) reduces the size and complexity of SpaceVPX. This paper describes a SpaceVPX-Lite board which uses SpaceWire and/or SpaceFibre for its backplane connections. The architecture of board is described along with its configuration options. An example application of the board as a wideband spectrometer is then described.

Index Terms—SpaceVPX, VITA, SpaceFibre, SpaceWire, Spacecraft Electronics, Radiation Tolerant, FPGA, RTG4, Spectrometer, FFT.

I. INTRODUCTION

There is a need for a standard backplane and rack for spacecraft avionics, to reduce development time and cost. However, each spaceflight system has its own requirements. Incorporating appropriate levels of redundancy is difficult and expensive in a standard system. Optimisations for mass, size and power savings also fight against a standard solution.

SpaceVPX-Lite is a draft standard (VITA 78.1) for spacecraft payload processing systems which defines a mechanical rack, an electrical interconnect including SpaceWire, a range of backplane profiles and a redundancy scheme. SpaceVPX and SpaceVPX-Lite have gone a long way to establishing an avionics standard or space applications.

SpaceWire is a widely used network technology for interconnecting payload data-handling equipment on-board a spacecraft. SpaceFibre is a new generation of SpaceWire spacecraft which has over ten times the performance and operates over both electrical and fibre optic media. It provides integrated quality of service and fault detection, isolation and recovery mechanisms which improve reliability and simplify redundancy.

This paper describes a SpaceVPX-Lite board which uses SpaceWire and/or SpaceFibre for its backplane connections. The architecture of board is described along with its configuration options. An example application of the board as a wideband spectrometer is then described.

II. SPACEVPX-LITE

SpaceVPX (VITA 78.0) is built on the ruggedized VPX standard [1]. It addresses the need for redundancy in spaceflight systems and focusses on conduction cooled racks. SpaceVPX replaces the VMEbus control-plane of VPX with SpaceWire, while retaining the versatility of a user defined data plane serial interconnect. SpaceVPX-Lite (VITA 78.1) reduces the size and complexity of SpaceVPX [2]. It focuses on 3U sized boards, restricts and rationalizes the possible backplane configurations of SpaceVPX and concentrates on the support of utility, control and data planes.

A SpaceVPX-Lite system is illustrated in Fig. 1. . It has four types of module or board that plug into a backplane or rack:

1. System controller module, which controls the operation of the other modules in the rack. There are two system controller modules, one nominal and one redundant.
2. Payload module, which is the main processing or data-handling functions. There is a maximum of six payload modules in the rack.
3. Power supply module, which provides power to the power switch modules for distribution to the other modules in the rack. There are two power supply modules, nominal and redundant.
4. Power switch module, which distributes power from the nominal or redundant power supply to the system controller and payload modules.

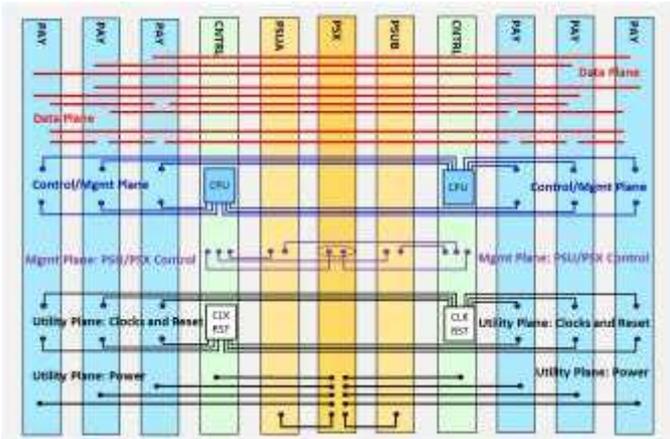


Fig. 1. SpaceVPX-Lite Backplane

SpaceVPX-Lite separates the backplane communications into four principal planes or functions:

1. Control plane, which is used to pass configuration, control and monitoring information between the system controllers and the payload modules. SpaceWire is used for the control plane links [3,4]. SpaceFibre may also be used for the control plane connections [5,6].
2. Data plane, which is used to pass information between the payload modules. The data plane supports several possible multi-Gbits/s serial technologies, for example SpaceFibre or Serial Rapid IO.
3. Utility plane, which is used to pass power, clock signals and control/status signals between the various modules in the SpaceVPX-Lite rack.
4. Management plane, which is used by the system controller to control and monitor the power supplies and power switches.

III. SPACEVPX-RTG4

STAR-Dundee has developed a SpaceVPX-Lite board to help with its work on the VITA 78.1 standard [7]. The board was used to test and evaluate various concepts, several of which have now been incorporated into VITA 78.1.

The SpaceVPX-RTG4 board is designed to be able to operate as a SpaceVPX-Lite controller or payload module. When operating as a payload module the board can be programmed to perform many different payload processing functions. An FMC type slot is available on the board for adding analogue IO functions.

A block diagram of the SpaceVPX-RTG4 board is shown in Fig. 2. The main component on the SpaceVPX-RTG4 board is a Microsemi RTG4 FPGA [8,9]. The Microsemi RTG4 is a radiation tolerant FPGA with extensive logic, memory, DSP blocks, and IO capabilities. It is inherently radiation tolerant, having triple mode redundancy built in. The RTG4 has a flash configuration memory incorporated in the device. In addition, the FPGA incorporates 16 SpaceWire clock-data recovery circuits and 24 multi-Gbits/s SerDes lanes to support high-speed serial protocols like SpaceFibre.

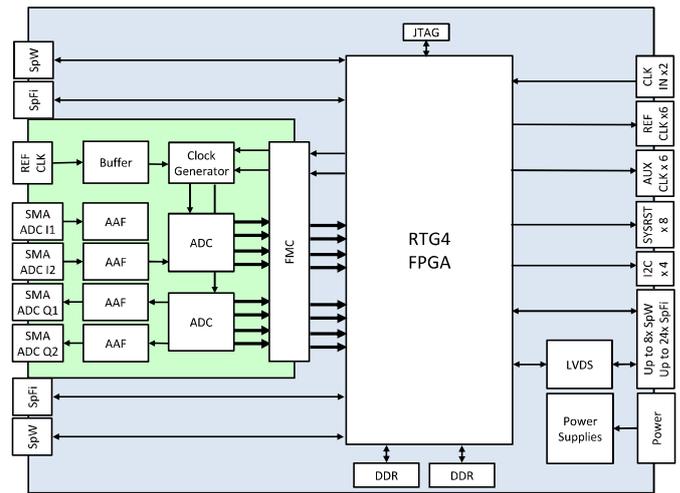


Fig. 2. SpaceVPX-RTG4 Board

The RTG4 FPGA is connected to two banks of DDR memory with EDAC protection. There are two SpaceWire and two single-lane SpaceFibre connections on the front panel. An FMC connector is included on the board so that analogue IO functions can be added to the SpaceVPX-RTG4. Fig. 2. shows a dual ADC board which is capable of sampling I and Q signals at 2.4 Gsamples/s with 8-bit resolution.

The SpaceVPX-RTG4 board can be configured as either a system controller or a payload module. Its backplane connections include a control plane comprising either six SpaceWire links or six SpaceFibre links and a data plane of six SpaceFibre links.

When configured as a system controller, as illustrated in Fig. 2. , the backplane connections comprise the following:

- Nominal and redundant system clock inputs which normally operated at 100 MHz;
- Radial clock outputs which distribute the system clock to each of the six payload boards using point-to-point LVDS connections;
- Nominal and redundant auxiliary clock inputs, which can be used for pulse per second or other timing signals;
- Radial auxiliary clock outputs which distribute the auxiliary clock to each of the six payload boards using point-to-point LVDS connections;
- Nominal and redundant system reset inputs;
- Radial system reset signals which distribute the system reset to each of the six payload boards;
- Up to four I2C buses which connect to the power supplies and power switch boards to control and monitor their operation;
- Six SpaceWire links, six single-lane SpaceFibre, or six dual-lane SpaceFibre links which connect to each payload module using point-to-point connections;
- Power input connections from the power switch boards.

When operating as a payload module the following connections are provided from the nominal and redundant system controllers:

- Nominal and redundant system clock inputs which normally operated at 100 MHz;
- Nominal and redundant auxiliary clock inputs, which can be used for pulse per second or other timing signals;
- Nominal and redundant system reset inputs;
- Nominal and redundant SpaceWire, single-lane SpaceFibre, or dual-lane SpaceFibre link.

In addition, there are power supply connections and SpaceFibre data plane connections between each of the payload boards.

A photograph of the SpaceVPX-RTG4 board is shown in Fig. 3. The board can be configured as a system controller or payload module using either SpaceWire or SpaceFibre as the backplane interconnect. This configurability is achieved using banks of resistors and capacitors, which can be seen to the left of the FPGA in Fig. 2. A dual ADC FMC board is fitted to the SpaceVPX-RTG4 board in Fig. 2.



Fig. 3. Photograph of SpaceVPX-RTG4 Board

IV. WIDEBAND SPECTROMETER

The SpaceVPX-RTG4 board has been used as the processing board in a microwave and Tera-Hertz radiometer being developed at Rutherford Appleton Laboratories [10][11].

The overall architecture of a spectrometer capable of analysing 8 GHz bandwidth is illustrated in Fig. 4. It is a hybrid spectrometer which comprises four individual wideband spectrometers (WBS V) which can each process 2 GHz bandwidth.

Each WBS V unit is a complete 2 GHz bandwidth spectrometer with I and Q analogue inputs, a 10 MHz (nominal) reference clock and a SpaceWire interface for configuration, control and monitoring and for retrieving the acquired power spectra. Several units can be interfaced to a SpaceWire router for connection via a single SpaceWire link to the spacecraft data-handling system. The SpaceWire router could be on the system controller board which controls all the WBS V payload modules and gathers science data from them. The resulting 8 GHz spectral data can be sent out of the nominal or redundant front panel SpaceWire or SpaceFibre interfaces of the system controller.

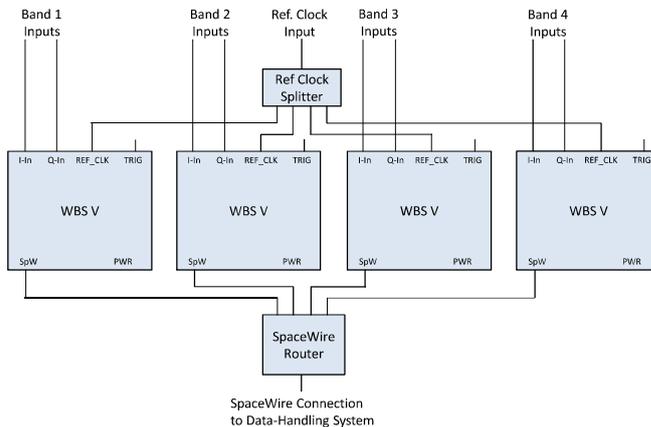


Fig. 4. Spectrometer Architecture

The architecture of an individual WBS V unit is illustrated in Fig. 2. and a photograph is shown in Fig. 5.



Fig. 5. WBS V Unit

The WBS V unit comprises two boards: the SpaceVPX-RTG4 board (shown in blue) and the FMC-3GHz-ADC board which is a dual ADC board (shown in green). The RTG4 FPGA contains the ADC interface, FFT, power spectrum, accumulation, control and monitoring and SpaceWire interface circuitry. The FMC board contains two high speed ADCs which are operated as an I and Q pair at 2.4 Gsamples/s.

The analogue I and Q signals from the RF front-end are connected to two SMA connectors on the FMC board. Each input to the ADCs is a single-ended (unbalanced) input through an edge mount SMA connector and a weak anti-aliasing filter. The anti-aliasing filter is for test purposes only, since an external anti-aliasing filter is expected for a flight unit.

The clock signals for the ADCs and FPGA are generated on board using a clock distributor and clock manager (CDCM) chip and a 1.2 GHz VCXO. The CDCM is locked to a 10 MHz reference clock from the FPGA. An external reference clock signal can also be used.

To operate the ADCs as an I and Q pair, it is necessary to ensure that the data outputs of the two ADCs are synchronised. This is done by resetting the data clocks of the two ADCs. This requires a Data CLK Reset signal which is synchronised to the 1.2 GHz clock requiring high speed logic.

A photograph of the dual ADC FMC board is shown in Fig. 6.



Fig. 6. Dual ADC FMC Board

Each ADC provides four de-interleaved data streams which are passed to the FPGA via the FMC connector. With a sample rate of 2.4 Gsamples/s the four data streams each operate at a data rate of 600 Msamples/s. These signals are transferred as low voltage differential signals (LVDS) to the FPGA. In total there are 128 data connections between the two ADCs and the FPGA. The four data streams are further de-interleaved within the FPGA.

A SpaceWire interface with support for the remote memory access protocol (RMAP) is provided for configuring, controlling and reading data from the WBS V. A trigger input or output interface is provided which may be used to trigger the operation of the WBS. A JTAG connector is provided on the SpaceVPX-RTG4 board for programming the Microsemi FPGA.

V. SPECTROMETER RESULTS

In this section the results of the WBS V are presented.

A. Development test set-up

A specially designed rack was used to house the WBS V during development and test, so that the two sides of the board were accessible to probe and monitor component operation. The operation of the WBS V spectrometer was tested using a signal generator connected to the inputs of the WBS V unit. The WBS V was controlled from a host computer via a SpaceWire link. The WBS V can be configured, controlled and monitored via SpaceWire and the results of data acquisition and processing can be retrieved and displayed.

B. Spectrometer results with signal generator input

Initially a complex 256-point FFT based spectrometer was implemented in the FPGA. The results of this spectrometer are illustrated in Fig. 7. showing a 1000 frame integration of a 541MHz I/Q signal using rectangular and Hann window functions. The largest peak is the input signal fundamental frequency and the three other large peaks are harmonics of the input signal fundamental. The noise floor is around 45 dB below the main signal.

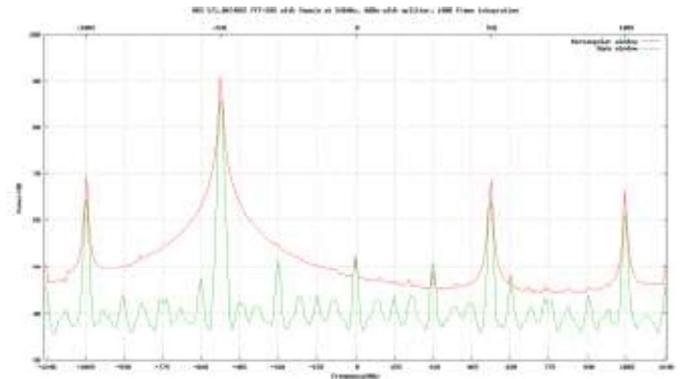


Fig. 7. “First Light” power spectrum using 256-Point FFT of 541MHz tone

Following the success of the 256-point FFT, the 1024-point FFT was implemented. Tests were made with a signal generator at difference frequencies, windowing functions and integration times. The results of this design with two different window functions and 1 million frames of integration (0.4 seconds) are shown in Fig. 8. The largest peak is the input signal fundamental frequency and the three other large peaks are harmonics of the input signal fundamental. The noise floor is around 56 dB below the main signal.

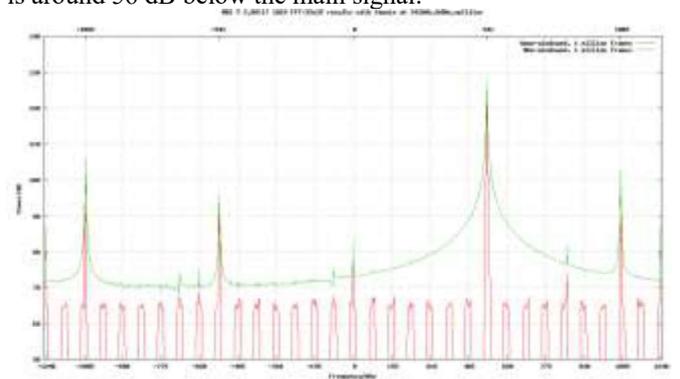


Fig. 8. Power spectrum using 1024-point FFT with 1 million frame integration

C. Spectrometer results with a 360GHz receiver and molecular spectra

The WBS V unit sealed in its case was tested at Rutherford Appleton Laboratories (RAL) with a 360GHz receiver using nitrous oxide and methanol at different pressures to provide real signal testing. A photograph of the test configuration and block diagram are shown in Fig. 9.

The gun diode was adjusted to select the local oscillator frequency around 90GHz. The precise setting depended on the molecular sample whose spectra was being captured. Note that both upper and lower side bands of the nominally 360GHz signal are captured by the WBS V. The targets were selected so that there were no lines in the upper side band or were much weaker than those in the lower side band (LSB).

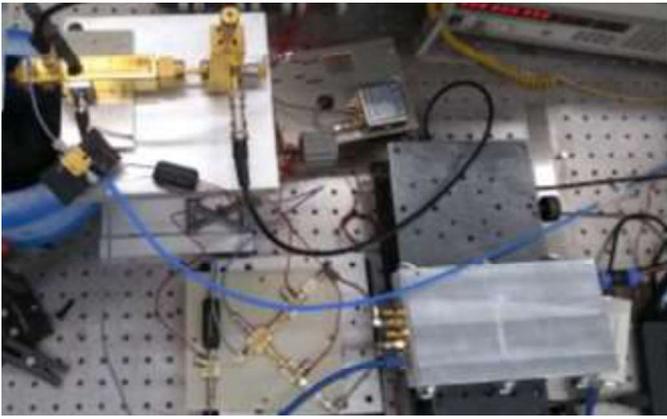


Fig. 9. WBS V with 360GHz receiver

The vacuum chamber into which the molecular samples were introduced is shown in Fig. 10. showing how it is observed by the 360GHz front-end and the location of the cold target (blue bucket). During the tests the marked movable flat mirror was rotated down to block the vacuum target from the front-end and to reflect the cold target instead. A corrugated black plastic insert was placed in front of the mirror to act as a hot (room-temperature) target.

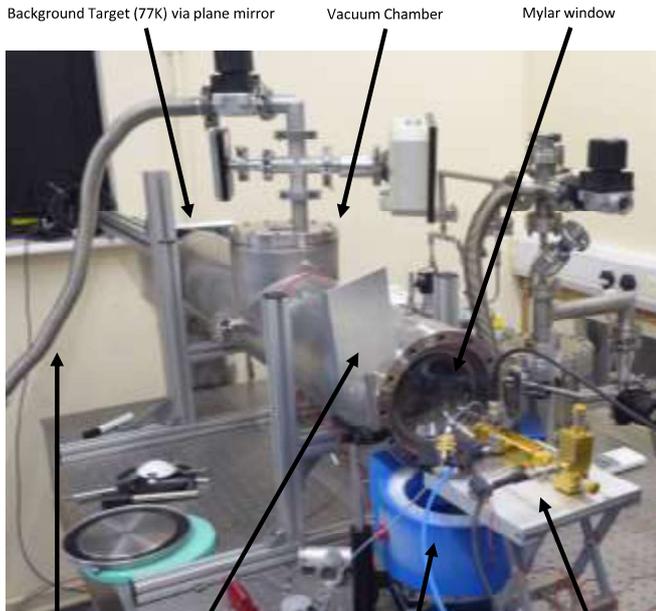


Fig. 10. Vacuum chamber with cold targets, flat mirror and front-end

To capture spectra the chosen molecular sample was introduced to the vacuum chamber and the pressure adjusted to the required upper target. The WBS V was used to capture three spectra, typically using two second integration periods with the Hann windowing function. The first spectra are of the cold (liquid nitrogen) target in the blue bucket, the second of the hot target, and the third of scene (the vacuum chamber). The ratio of the difference in the power of the hot and cold targets (in each FFT bin) relative to the difference in their temperatures (nominally 291K and 77K respectively) allows the power in each bin of the spectrum of the vacuum target to

be converted into a brightness temperature; the power of the cold target in each bin provides the temperature reference. Between each capture the flat mirror had to be moved and positioned by hand so there are likely to be differences in the hot/cold results each time the spectra were captured.

A plot of a nitrous oxide sample showing the effects of pressure on the line width are shown in Fig. 11. The spectra were captured using the WBS V.

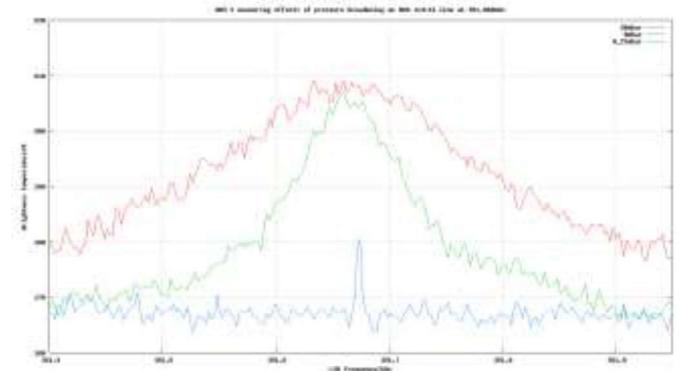


Fig. 11. WBS V spectra of nitrous oxide line at different pressures

VI. CONCLUSIONS AND FUTURE WORK

The SpaceVPX and SpaceVPX-Lite standards have been introduced and the design of a SpaceVPX-Lite board which uses SpaceWire and/or SpaceFibre for its backplane connections has been described. SpaceFibre has been included in the SpaceVPX and SpaceVPX-Lite standards as control plane or data plane interconnect. The SpaceVPX-Lite standard is in the process of being completed.

An example application of the Space-VPX as a wideband spectrometer has been outlined. It is intended to extend the bandwidth of STAR-Dundee's spectrometer technology to 8 GHz.

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REFERENCES

- [1] VITA, “SpaceVPX System”, ANSI/VITA 78.00-2015, April 2015.
- [2] Scott Goedeke, et al. “SpaceVPX Lite, Lightweight SpaceVPX Systems Specification”, VITA 78.1, Draft revision 2.3, VITA, 14 July 2016.
- [3] ECSS Standard ECSS-E-ST-50-12C, “SpaceWire, Links, Nodes, Routers and Networks”, Issue 1, European Cooperation for Space Data Standardization, July 2008, available from <http://www.ecss.nl>.
- [4] S. Parkes, “SpaceWire Users Guide”, ISBN: 978-0-9573408-0-0, STAR-Dundee, 2012, available from <https://www.star-dundee.com/knowledge-base/spacewire-users-guide> (last visited 21st April 2018).
- [5] S. Parkes, A. Ferrer Florit and A. Gonzalez Villafranca, “SpaceFibre Standard”, Draft K2, University of Dundee, December 2017.
- [6] S. Parkes et al, “SpaceFibre: Multi-Gigabit/s Interconnect for Spacecraft On-board Data Handling”, IEEE Aerospace Conference, Big Sky, Montana, 2015.
- [7] S. Parkes et al, “A Prototype SpaceVPX Lite (VITA 78.1) System using SpaceFibre for Data and Control Plane”, IEEE Aerospace Conference, Big Sky, Montana, 2017.
- [8] S. Parkes et al, “SpaceWire and SpaceFibre on the Microsemi RTG4 FPGA”, IEEE Aerospace Conference, Big Sky, Montana, 2016.
- [9] Microsemi, “DS0131 Datasheet RTG4 FPGA”, <https://www.microsemi.com/.../135193-ds0131-rtg4-fpga-datasheet>. Last visited 21st April 2018.
- [10] S. Parkes et al, “A Wideband Spectrometer in the Microsemi RTG4 FPGA”, Data Systems in Aerospace (DASIA) Conference, Oxford, UK, May 2018.
- [11] S.P. Rea, et al, “The Low-Cost Upper-Atmosphere Sounder (LOCUS)”, 26th International Symposium on Space Terahertz Technology, Cambridge, MA, 16-18 March 2015.