

# Hi-SIDE: Monitoring, Control and Test Software in a SpaceFibre Network

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**Abstract**—The aim of the Hi-SIDE project [1] was to develop and demonstrate technologies that enable future high-speed on-board data-handling systems. The Hi-SIDE demonstration system consisted of several elements including a SpaceFibre Camera and an instrument simulator generating high data-rate payload data; two processing elements providing compression and encryption; a PC-Based Mass-Memory providing onboard storage and playback functions; two downlink systems providing Radio Frequency (RF) and optical links; a File-Protection Scheme (FPS) to protect against errors or outages in the optical downlink; and a Control Computer used to monitor and control the other elements.

Each of the Hi-SIDE instruments, processing, storage, and downlink elements were interconnected via SpaceFibre using the STAR-Tiger SpaceFibre [2] Routing Switch; and monitored, configured and controlled by the Control Computer.

As part of the Hi-SIDE project, software was designed and developed by STAR-Dundee to monitor and control the other elements. In addition, to demonstrate the high data-rate capabilities of the processing and downlink elements in the Hi-SIDE system, software was designed and developed by STAR-Dundee to support the transmission, storage, and playback of files encoded in Consultative Committee for Space Data Systems (CCSDS) Space Packet Protocol (SPP) [3] and Transfer Frame (TF) [4] packets at data rates of over 10 Gbit/s.

This paper describes the monitoring, control and test software that was developed by STAR-Dundee within the Hi-SIDE project and provides performance results.

**Keywords**—SpaceFibre, Hi-SIDE, On-Board Data-Handling

## I. INTRODUCTION

The High-Speed Data-Chain (HSDC) system developed in the Hi-SIDE project demonstrates the full on-board data-chain consisting of several elements. The elements included two instruments, two processing systems, a PC-Based Mass-Memory, Radio Frequency (RF) and optical downlinks, a File Protection Scheme (FPS) used to protect against errors and outages in the optical downlink, and a Control Computer used to monitor and control the other elements. The following sections provide a brief description of these elements.

### A. Instruments

The two instruments, designed and developed by STAR-Dundee, were a SpaceFibre Camera used to capture and transmit images, and an instrument simulator used to transmit files. Each instrument used two protocols to encapsulate data. Firstly, user data items e.g., image frames or files, were

segmented and encoded in CCSDS SPP packets. To identify the start, middle and end of user data items, the sequence flags within the SPP packet primary header were used. Each data source in the HSDC system was assigned its own SPP Application Identifier (APID) to distinguish between different data products. Secondly, the SPP packets were encapsulated in Payload Data Encapsulation Protocol (PDEP) packets which contained the path and logical addresses, the Protocol Identifier (PID), the Source Logical Address (SLA) and a sequence number. The PDEP format was in accordance with the ECSS-E-ST-50-51C SpaceWire Protocol Identification standard [5].

A photograph of the SpaceFibre Camera connected to the SpaceFibre network is shown in Figure 1.

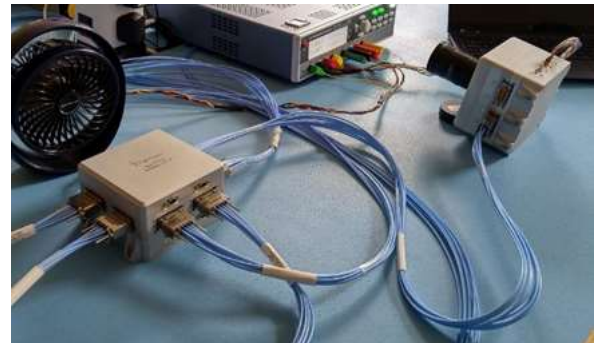


Fig. 1. SpaceFibre Camera

In Figure 1, the photograph shows the SpaceFibre Camera at the top-right connected to the STAR-Tiger SpaceFibre Routing Switch at the bottom-left using a quad-lane Elara-to-Elara SpaceFibre cable assembly. The SpaceFibre link was running at a lane rate of 6.25 Gbit/s, providing a link signalling rate of 25 Gbit/s.

The instrument simulator consisted of a STAR-Ultra PCI Express (PCIe) board [6] running on a standard desktop Personal Computer (PC) with a software application used to receive commands from the Control Computer, encapsulate files in SPP and PDEP packets and transmit them over the SpaceFibre network.

A photograph of the STAR-Ultra PCIe board is shown in Figure 2.



Fig. 2. STAR-Ultra PCIe

In Figure 2, the photograph shows the front-panel of the STAR-Ultra PCIe board. The board has two quad-lane SpaceFibre interfaces that use Quad Small Form-Factor Pluggable (QSFP) connectors. The SpaceFibre lanes can run at a signalling rate of 6.25 Gbit/s, providing a link signalling rate of 25 Gbit/s. In the HSDC system, the instrument simulator was connected to the STAR-Tiger SpaceFibre Routing Switch using a dual-lane QSFP-to-Elara cable assembly, providing a link signalling rate of 12.5 Gbit/s.

#### B. Data Processors

The two data processors included in the HSDC system were the Data Compression Module used to compress files encapsulated in SPP and PDEP packets, and the High-Performance Data-Processor (HPDP) used to compress or encrypt files encapsulated in SPP and PDEP packets.

The Data Compression Module [7] was produced by Airbus Defence and Space and included the Hyperspectral Compression Engine (HCE) developed by the National and Kapodistrian University of Athens (NKUA).

A photograph of the Data Compression Module connected to the SpaceFibre network is shown in Figure 3.

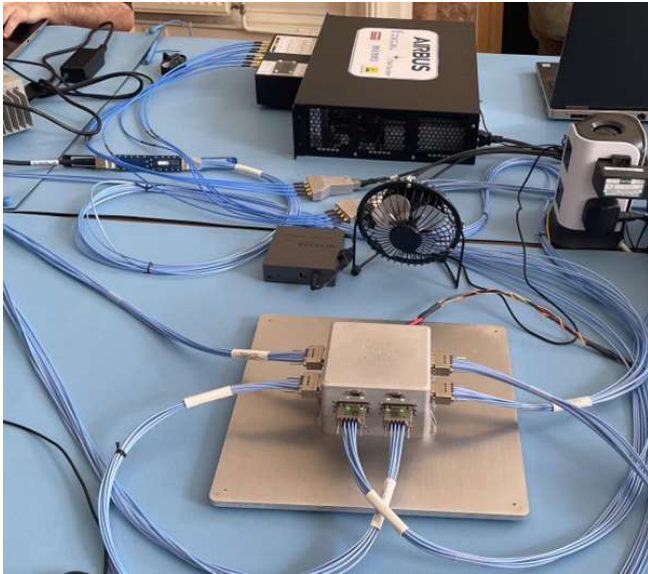


Fig. 3. Data Compression Module

In Figure 3, the photograph shows the Data Compression Module at the top connected to the STAR-Tiger SpaceFibre Routing Switch at the bottom using various cables and adaptors to convert between Sub Miniature Push-on Micro (SMPM) and Elara.

The HPDP [8] was produced by Integrated Systems Development (ISD) and included algorithms to perform data compression and encryption.

A photograph of the HPDP connected to the SpaceFibre network is shown in Figure 4.



Fig. 4. High-Performance Data-Processor

In Figure 4, the photograph shows the HPDP connected to the SpaceFibre network. The HPDP was connected to the STAR-Tiger SpaceFibre Routing Switch using various cables and adaptors to convert between Sub Miniature Push-On (SMP) and Elara.

#### C. PC-Based Mass-Memory

The PC-Based Mass-Memory, designed and developed by STAR-Dundee, consisted of a STAR-Ultra PCIe board running in a standard desktop PC with a software application used to receive commands from the Control Computer; receive and store data sent by the instruments or data processors; and playback data to the data processors or downlink elements.

The PC-Based Mass-Memory and its software are described in more detail in Section III.

#### D. Downlinks

The two downlink elements included in the HSDC system were the RF Downlink used to transmit data to ground using two Ka-band transmitters, and the Optical Downlink used to transmit data to ground using a laser communication terminal.

The RF Downlink [9] was produced by TESAT and included a 2 W Ka-band Solid-State Power Amplifier (SSPA) developed by ERZIA, and a demodulator developed by Kongsberg for the ground segment.

A photograph of the RF Downlink connected to the SpaceFibre network is shown in Figure 5.

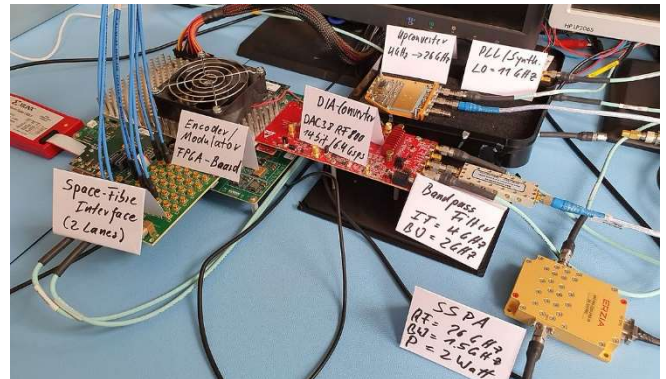


Fig. 5. RF Downlink [11]



In Figure 5, the photograph shows the RF Downlink connected to the SpaceFibre network at the left. The RF Downlink was connected to the STAR Tiger Routing Switch using various cables and adaptors to convert between SMP and Elara.

The Optical Downlink [10] was produced by the German Aerospace Center (DLR) in collaboration with TESAT and included a File Protection Scheme (FPS) used to protect against errors and outages in the optical link.

#### E. Control Computer

The Control Computer, developed by STAR-Dundee, consisted of a STAR-Ultra PCIe board running in a standard desktop PC with a software application used to monitor and control the other elements.

The Control Computer and its software are described in more detail in Section IV.

## II. TEST EQUIPMENT SOFTWARE

Early in the Hi-SIDE project, the STAR-Ultra PCIe board was designed and developed by STAR-Dundee to provide the Hi-SIDE partners with a SpaceFibre interface board to use during the design and development of their own elements.

In addition to the STAR-Ultra PCIe board, supporting test applications were designed, implemented, and provided to the Hi-SIDE partners in order to simplify integration later in the project.

The following sections describe the STAR-Ultra PCIe software and the supporting test applications.

#### A. STAR-Ultra PCIe Software

The software that was developed to support the STAR-Ultra PCIe board included:

- A high-performance PCIe driver used to transmit and receive data between the host PC and the board.
- A device configuration application used to configure the SpaceFibre lanes and links.
- A link analysis application used to support capturing and visualisation of SpaceFibre traffic.

The STAR-Ultra PCIe device driver was integrated with STAR-Dundee's STAR-System [11] software suite. This integration allowed the STAR-Ultra PCIe board to be used with the existing STAR-System applications and Application Programming Interfaces (APIs).

The performance objective for the STAR-Ultra PCIe was to be able to transmit and receive packets at over 10 Gbit/s in both directions simultaneously in order to support the overall 10 Gbit/s performance objective of the Hi-SIDE project. As described in Section III, this objective was achieved, for example, in applications such as the PC-Based Mass-Memory software and, as described in Section II.B, the Hi-SIDE File Transmit and File Receive applications.

#### B. Test Applications

To support the development of the Hi-SIDE elements, and to ensure that protocols were implemented consistently across the project, STAR-Dundee developed test applications used with the STAR-Ultra PCIe board.

The Hi-SIDE File Transmit application was used to encode one or more files in the protocols used in the Hi-SIDE

project. For example, files could be encoded in SPP and PDEP packets for transmission to a processing element, or in SPP, TF and TFEP packets for transmission to a downlink element.

A screenshot of the Hi-SIDE File Transmit application is shown in Figure 6.

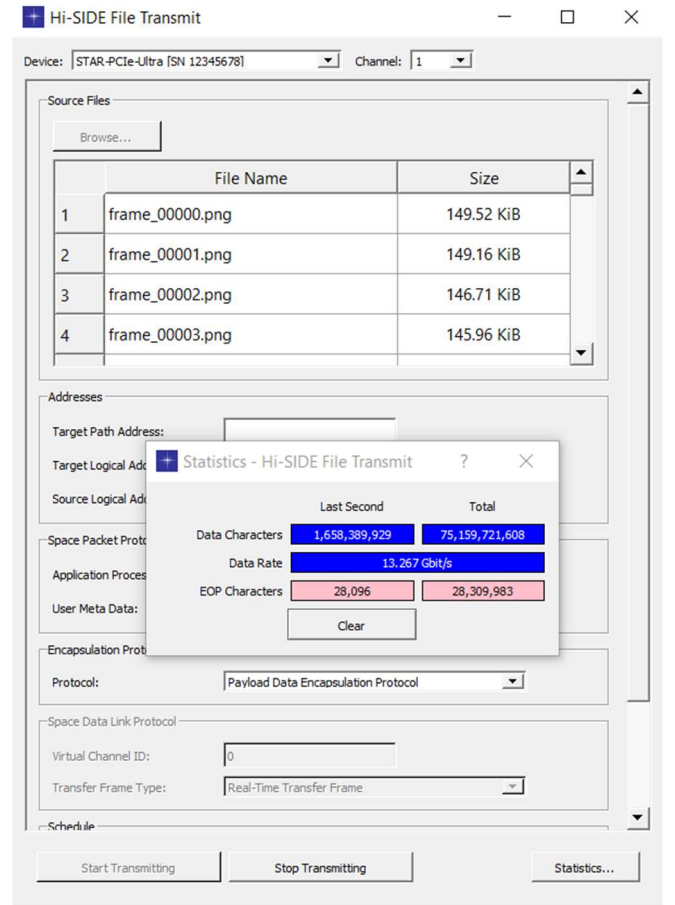


Fig. 6. Hi-SIDE File Transmit

In Figure 6, the screenshot shows the Hi-SIDE File Transmit application sending a list of image files encoded in SPP and PDEP packets at approximately 13 Gbit/s.

The Hi-SIDE File Receive application was used to receive, decode and optionally store files encoded in SPP and PDEP; or SPP, TF, and TFEP packets.

A screenshot of the Hi-SIDE File Receive application is shown in Figure 7.

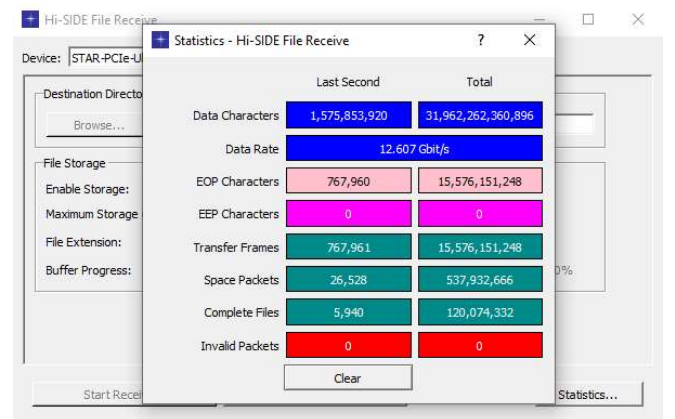


Fig. 7. Hi-SIDE File Receive

In Figure 7, the screenshot shows the Hi-SIDE File Receive application in operation, receiving a list of files encoded in SPP, TF and TFEP packets at approximately 12.5 Gbit/s, or over 750000 transfer frames per second.

### III. PC-BASED MASS-MEMORY SOFTWARE

The PC-Based Mass-Memory was a software implementation of a block-based file system used to receive, store and playback files.

For receiving and storing files, instruments or processing elements transmit files encapsulated in SPP and PDEP packets to the PC-Based Mass-Memory.

For playing back files, the Control Computer commands the PC-Based Mass-Memory to playback a stored file to a receiver in either PDEP or TFEP encoding modes.

The PC-Based Mass-Memory software ran on a desktop PC with the following specifications:

- Intel Core i9-9900K 3.6 GHz 8-Core CPU
- 128 GB Corsair Vengeance LPX 3200 MHz DDR4
- 2 x 500 GB Samsung 970 EVO Plus M.2 NVMe SSD
- Gigabyte Z390 UD ATX Motherboard

The PC-Based Mass-Memory's STAR-Ultra PCIe board was connected to the SpaceFibre Routing Switch via a quad-lane SpaceFibre interface with eight virtual channels. The SpaceFibre lanes ran at a signalling rate of 6.25 Gbit/s, providing a link signalling rate of 25 Gbit/s

#### A. Storing Data

When packets were received at the PC-Based Mass-Memory, they were filtered and stored in files based on the APID in the SPP primary packet header. A diagram illustrating this process is shown in Figure 8.

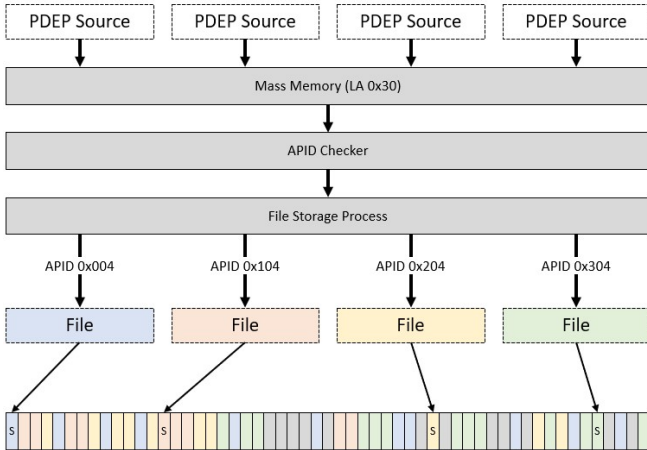


Fig. 8. PC-Based Mass-Memory

In Figure 8, there are four PDEP sources e.g., instruments or processing elements. The PDEP sources send payload data encapsulated in SPP and PDEP packets to the PC-Based Mass-Memory with logical address 0x30. When the packets are received, the PDEP and SPP packets are validated and the APID is extracted. If the APID is currently mapped to a file, the user data is passed to the file storage process. Finally, the file storage process appends the user data to the relevant file, which consists of a linked list of one or more non-contiguous blocks in the file system.

#### B. Playing Back Files

To playback a stored file, the Control Computer sends a playback file command to the PC-Based Mass-Memory with several parameters including the file name of the file to play back, the target logical address, the virtual channel on which to play back the file, and the requested encoding mode.

In PDEP encoding mode, the stored SPP packets are retrieved from the file system, encapsulated in PDEP headers, and transmitted to the target. In TFEP encoding mode, the stored SPP packets are retrieved from the file system, segmented and encoded in TF packets, encapsulated in TFEP headers, and transmitted to the target.

#### C. Control Interface

The control interface for the PC-Based Mass-Memory was a reusable software Remote Memory Access Protocol (RMAP) [12] target that was developed during the Hi-SIDE project. For example, there were commands to create files, delete files, map APIDs to files, unmap APIDs from files, playback files encoded in PDEP or TFEP encoding modes, and save and load files from local storage.

#### D. Performance

Prior to the demonstration, the performance of the PC-Based Mass-Memory was verified in three test scenarios: storage, playback, and simultaneous storage and playback. To measure and visualise performance, VC utilisation parameters in the STAR-Tiger SpaceFibre Routing Switch for the VCs going in and out of the PC-Based Mass-Memory were sampled by the control software and plotted over time during the tests.

A performance chart for the storage test scenario is provided in Figure 9.

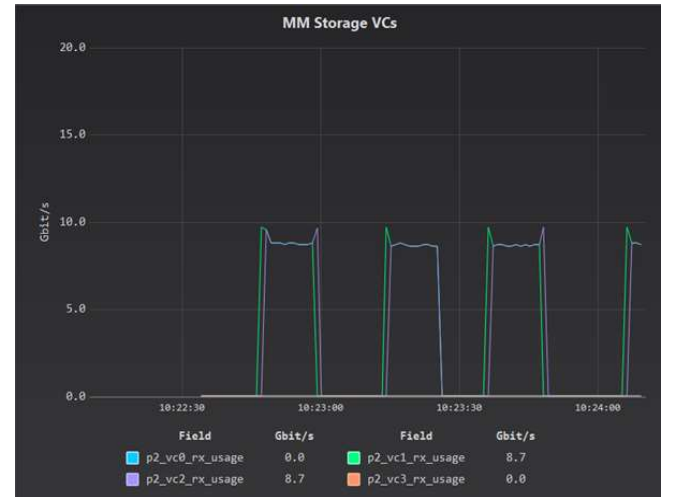


Fig. 9. Storage Performance

In Figure 9, the chart shows the data rates going into the PC-Based Mass-Memory during file storage operations from two PDEP sources sending files on VCs 1 and 2. As shown in the chart, the performance is approximately 8.5 Gbit/s on each VC, or approximately 17 Gbit/s in total on the link.

A performance chart for the playback test scenario, using PDEP encoding mode, is provided in Figure 10.

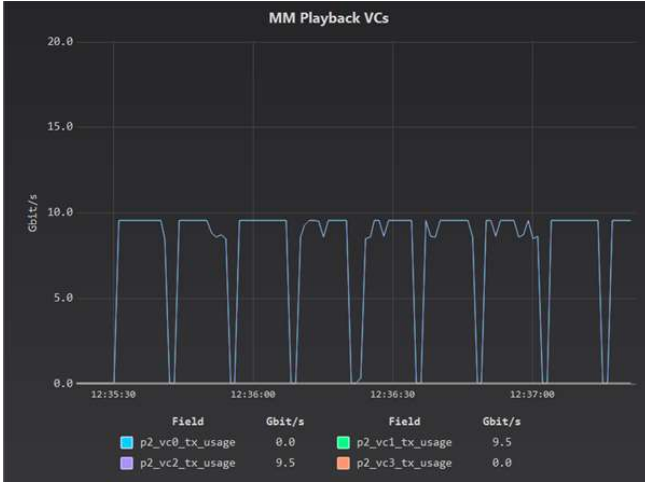


Fig. 10. Playback Performance (PDEP Mode)

In Figure 10, the chart shows the data rates coming out of the PC-Based Mass-Memory during file playback operations in PDEP encoding mode to two receivers. The playback operations are using VC 1 and VC 2 and as shown in the chart, the performance is approximately 9.5 Gbit/s on each VC, or approximately 19 Gbit/s in total on the link.

A performance chart for the playback test scenario, using TFEP encoding mode, is provided in Figure 11.

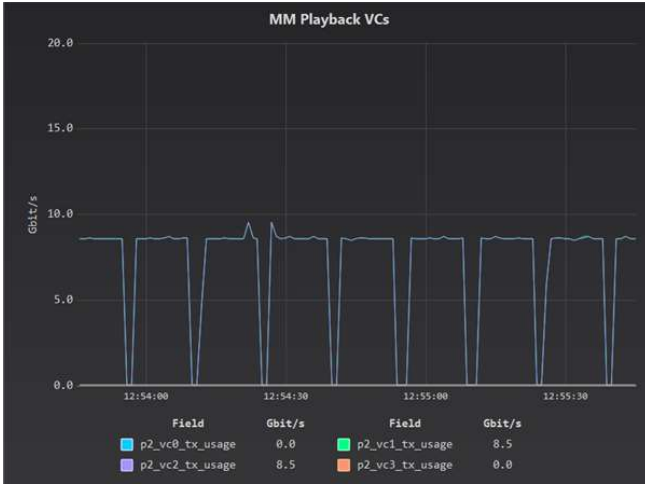


Fig. 11. Playback Performance (TFEP Mode)

In Figure 11, the chart shows the data rates coming out of the PC-Based Mass-Memory during file playback operations in TFEP encoding mode to two receivers. In this case, the performance is lower due to the overhead of TFEP encoding and the performance is approximately 8.5 Gbit/s on each VC, or approximately 17 Gbit/s in total on the link.

A performance chart for the simultaneous storage and playback test scenario is provided in Figure 12.



Fig. 12. Simultaneous Storage and Playback Performance

In Figure 12, the chart shows the data rates going in and out of the PC-Based Mass-Memory during four simultaneous file storage and playback operations. The four plots are showing the two VCs used to receive data for storage, and the two VCs used to playback files. As shown in the chart, the data rate is approximately 12.5 to 13 Gbit/s in each direction, or an aggregate of 25 to 26 Gbit/s.

During the execution of these tests, the control software was used to send commands to the PC-Based Mass-Memory to create the files, map APIDs to the files, and playback the stored files. It was also used to monitor and visualise the performance by sampling the VC utilisation parameters within the STAR-Tiger SpaceFibre Routing Switch and display the performance charts.

#### IV. CONTROL SOFTWARE

The control software, referred to as the Hi-SIDE Monitoring and Control System (MCS), ran on the Control Computer and was responsible for configuring, monitoring, and controlling the other elements during the demonstration.

Specifically, it performed the following tasks:

- Initialisation of the SpaceFibre network, including routing table configuration, setting the lane signalling rates, and link configuration.
- Initialisation of the HSDC elements, where necessary.
- Execution of control scripts used to automate the demonstration scenarios via a Python-based [13] scripting system.
- Monitoring and visualisation of relevant parameters available in the RMAP target memory of the HSDC elements.

##### A. Software Layers

A block diagram illustrating the layers of the Hi-SIDE MCS software is provided in Figure 13.

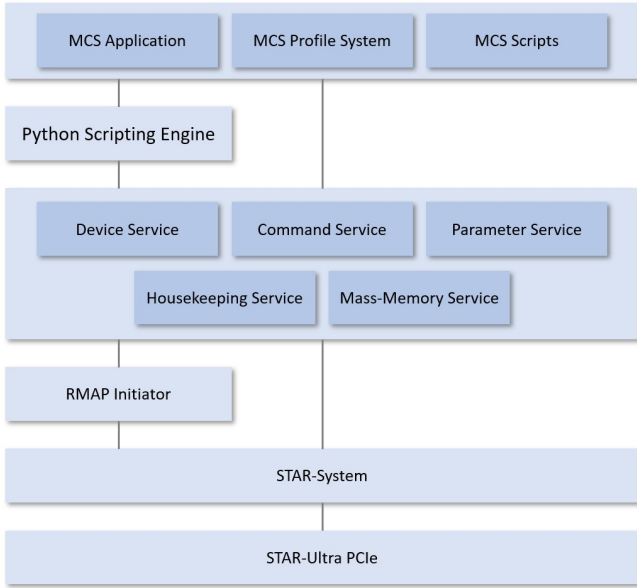


Fig. 13. Hi-SIDE MCS Layers

The top layer included the MCS Application, providing the graphical user interface; the MCS Profile System, used to describe devices in text file format; and the MCS Scripts, which were Python scripts used to automate control of the other elements.

The next layer provided the Python Scripting Engine, which included an embedded Python interpreter and Python wrappers around the services layer below.

The services layer provided the core functionality such as device management, scheduling and executing commands, parameter management, housekeeping, and interacting with the PC-Based Mass-Memory.

The RMAP Initiator was the interface to the SpaceFibre network and was used by the services to send RMAP commands to the other elements and process the corresponding RMAP replies.

Finally, the bottom two layers included STAR-System and the STAR-Ultra PCIe, as described in Section II.

### B. MCS Profiles

The MCS Profile file format was designed to allow each HSDC element to be described electronically so that the control software was aware of how to communicate with the element, the commands available to control the element, and the parameters available to monitor the element.

MCS Profiles were text files processed by the control software and containing the element's characteristics. Each MCS Profile contained an element's name, command path, reply path, and key, used to determine how to access an element's RMAP target memory. Following this, an element was described in terms of memory areas, registers, fields, and buffers. Each field was assigned one of the built-in types such as integer or hexadecimal, or a user-defined type created to translate between raw values and meaningful strings. In addition, optional monitoring information could be provided such as lower and upper limits or expected values.

The MCS Profiles were then processed when a project was opened to populate the library of remote devices, commands, and parameters available to the services.

### C. Parameter Tables and Charts

After processing the MCS Profiles for each HSDC element, any parameters within an element's RMAP target memory were available to be added to the housekeeping plan, meaning they were then sampled periodically and could be displayed in parameter tables or charts.

An example of a parameter table is shown in Figure 14.

SpaceFibre Link Errors - Hi-SIDE Monitoring and Control System

Field	Device	Sample Time	Lower	Upper	Expected	Actual
p1_link_err	STAR-Tiger	15:14:37.510	N/A	N/A	0	NO ERRORS
p2_link_err	STAR-Tiger	15:14:37.511	N/A	N/A	0	NO ERRORS
p3_link_err	STAR-Tiger	15:14:37.512	N/A	N/A	0	NO ERRORS
p4_link_err	STAR-Tiger	15:14:37.513	N/A	N/A	0	NO ERRORS
p5_link_err	STAR-Tiger	15:14:37.514	N/A	N/A	0	NO ERRORS
p6_link_err	STAR-Tiger	15:14:37.514	N/A	N/A	0	NO ERRORS
p7_link_err	STAR-Tiger	15:14:37.515	N/A	N/A	0	NO ERRORS
p8_link_err	STAR-Tiger	15:14:37.516	N/A	N/A	0	NO ERRORS
p9_link_err	STAR-Tiger	15:14:37.517	N/A	N/A	0	NO ERRORS
p10_link_err	STAR-Tiger	15:14:37.507	N/A	N/A	0	NO ERRORS

Fig. 14. Parameter Table

In Figure 14, the screenshot shows a parameter table containing the link error parameters for the SpaceFibre links within the STAR-Tiger Routing Switch. For these parameters, they had an expected value of 0, so they were displayed in green when at the expected value, and red when they were not.

Multiple examples of charts were provided in Section III, as the Hi-SIDE MCS software was used during the PC-Based Mass-Memory's performance verification testing.

### D. MCS Scripts

For the final demonstration, several Python scripts were created to automate the demonstration scenarios using the Python wrappers around the core services.

A diagram illustrating the Hi-SIDE MCS's scripting system is shown in Figure 15.

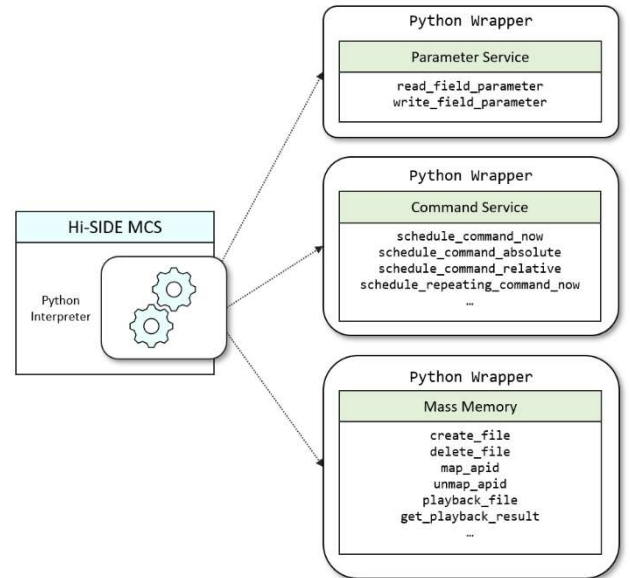


Fig. 15. MCS Scripting System

In Figure 15, the diagram shows some of the core services on the right, with each service having a Python wrapper. A Python Interpreter was then embedded in the Hi-SIDE MCS



application and used to execute scripts that called the Python wrappers.

The final demonstration included the following scenarios:

- SpaceFibre Camera: Storage and Playback
- Instrument Simulator: Storage and Playback
- Compressor: Playback, Compression and Storage
- HPDP: Playback, Encryption and Storage
- RF Downlink and Demodulator: Playback
- File Protection Scheme

Scripts were created to automate the scenarios listed above, with the main script demonstrating the SpaceFibre Camera, Instrument Simulator, Data Compression Module, HPDP, and RF Downlink scenarios simultaneously.

While the demonstration scenarios were being executed, the Hi-SIDE MCS application was periodically sampling the VC utilisation registers within the STAR-Tiger Routing Switch in order to visualise the data flows going in and out of the PC-Based Mass-Memory on the various Virtual Networks.

A chart showing the traffic going to the PC-Based Mass-Memory for storage is provided in Figure 16.

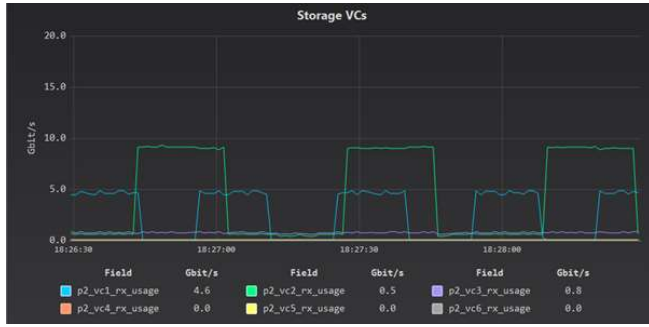


Fig. 16. Demonstration (Storage)

In Figure 16, the chart is showing data rates plotted over time for the VCs going into the PC-Based Mass-Memory. In this chart, the following data flows are shown:

- VC 1 (blue line):
  - SpaceFibre Camera sending 8 GB of images to the PC-Based Mass-Memory for storage.
- VC 2 (green line):
  - Instrument Simulator sending 16 GB of data to the PC-Based Mass-Memory for storage.
  - Compressor sending one half of the compressed data to the PC-Based Mass-Memory for storage.
- VC 3 (purple line):
  - Compressor sending the other half of the compressed data to the PC-Based Mass-Memory for storage.

When these operations overlap, the total data rate of traffic being stored in the PC-Based Mass-Memory simultaneously is over 13 Gbit/s (SpaceFibre Camera is approximately 4.5 Gbit/s, Instrument Simulator is approximately 9 Gbit/s, Compressor is approximately 0.5 Gbit/s per output stream).

A chart showing the traffic coming out of the PC-Based Mass-Memory during playback is provided in Figure 17.

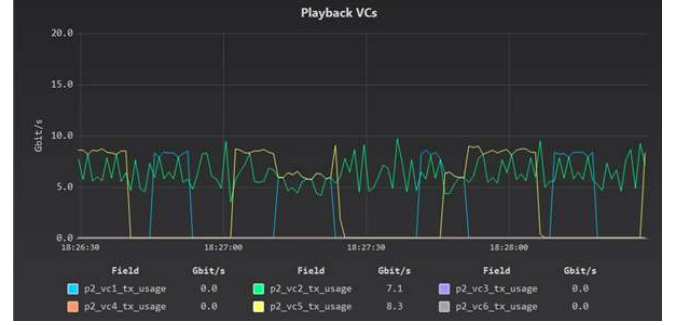


Fig. 17. Demonstration (Playback)

In Figure 17, the chart is showing data rates plotted over time for the VCs going out of the PC-Based Mass-Memory used to playback data. In this chart, the following data flows are shown:

- VC 1 (blue line):
  - Playback of 8 GB of SpaceFibre Camera images in PDEP mode to an Image Display receiver.
- VC 2 (green line):
  - Playback of uncompressed hyperspectral images in PDEP mode to the Compressor.
- VC 5 (yellow line):
  - Playback of 16 GB of Instrument Simulator data in TFEP mode to a receiver.

Due to the bursts of uncompressed hyperspectral images to the Compressor, it's more difficult to tell the total data rate of traffic when operations overlap. However, they overlap just to the left of the centre of the chart and the three playback operations are approximately 4.5 to 5.5 Gbit/s each, resulting in a total data rate of at least 13 Gbit/s.

## V. CONCLUSIONS

During the Hi-SIDE project, STAR-Dundee developed various software drivers, APIs, and applications, designed to support the partners on the project, monitor and control the demonstrator, and meet the performance objectives.

At the lowest level, the STAR-Ultra PCIe board provided the interface to the SpaceFibre network, used by the partners during the development of their own elements, and in the final demonstration by the Instrument Simulator, PC-Based Mass-Memory, and Control Computer, which were developed by STAR-Dundee.

To support the STAR-Ultra PCIe board, a high-performance PCIe driver was developed for Windows and Linux operating systems and integrated with the STAR-System software suite.

On top of the STAR-Ultra PCIe driver and STAR-System, software was developed to transmit and receive files encoded in CCSDS SPP and TF protocols; store and playback files in the PC-Based Mass-Memory; and monitor and control the HSDC elements in the Control Computer.

The Hi-SIDE project culminated in the integration and demonstration of the HSDC elements, which took place

successfully in June 2022 at STAR-Dundee's office in Dundee, Scotland.

#### ACKNOWLEDGEMENT

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