Testing SpaceFibre in Orbit: the OPS-SAT and NORBY Technology Demonstrators

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***Abstract*— SpaceFibre (ECSS-E-ST-50-11C) is a technology specifically designed for use on-board spacecraft that provides point to point and networked interconnections at Gigabit rates with Quality of Service (QoS) and Fault Detection, Isolation and Recovery (FDIR). SpaceFibre is backwards compatible with SpaceWire (ECSS-E-ST-50-12C), allowing existing SpaceWire equipment to be incorporated into a SpaceFibre network without modifications at the packet level. As part of its worldwide adoption by the aerospace industry, experiments are being developed to demonstrate the capabilities and performance of SpaceFibre in space.**

This article presents the results of two collaborations of STAR-Dundee, one with the European Space Agency (ESA) OPS-SAT team and one with Thales Alenia Space (TAS) to develop SpaceFibre technology demonstrators. These consist of an implementation of the STAR-Dundee SpaceFibre Interface IP core as part of the spacecraft payload. The aim of these collaborations was to increase the technology readiness level (TRL) of SpaceFibre by demonstrating an operational SpaceFibre link in orbit, providing examples of flying heritage for the technology.

The first collaboration is an implementation of a SpaceFibre link in a commercial off-the-shelf (COTS) device hosted in the OPS-SAT spacecraft developed by ESA. The entire SpaceFibre was implemented in the FPGA (Intel Cyclone V) and it was controlled and monitored from a CPU. The experiment generates and sends data in loopback using different virtual channels in the link, and the received data is subsequently checked for errors. During the activity SpaceFibre is continuously being monitored looking for issues in the link.

The second collaboration was with TAS in the NORBY mission. In this activity SpaceFibre is also implemented in a commercial FPGA, and the monitoring and control of the link is done by a LEON3 processor. Similarly, this activity also uses data generators to send data in loopback and the received data is checked for errors.

The results of both activities were successful. All the data transmitted were received with no errors, showing that SpaceFibre links implemented even in commercial FPGAs can reliably operate in space.

Keywords—SpaceFibre, OPS-SAT, NORBY

I. Introduction

SpaceFibre (SpFi) is a very high-speed serial link designed specifically for use onboard spacecraft [1]. It was released as an ECSS standard in 2019. SpFi can operate over fibre-optic and electrical cable, and aims to complement the capabilities of the widely used SpaceWire (SpW) onboard networking standard [2]. It improves the data rate by a factor of more than 10, reducing the cable mass and providing galvanic isolation. SpFi provides a coherent QoS mechanism able to support bandwidth reserved, scheduled and priority-based qualities of service. It also substantially improves the FDIR capabilities compared to SpW.

SpFi is being adopted worldwide by the aerospace industry and as part of this adoption, new experiments are developed to demonstrate its capabilities and performance in real space environments. This paper describes two experiments designed for two different missions that implemented and run a demonstrator design of the SpFi interface in orbit.

A. OPS-SAT Mission

OPS-SAT is a 3U CubeSat (Fig. 1) launched by ESA on December 18, 2019 [3]. It is the first nanosatellite to be directly owned and operated by ESA. OPS-SAT includes a system on module (SoM) platform containing state-of-the-art semiconductor technologies. The platform is called satellite experimenter processing platform (SEPP) and can take control over of the whole satellite and doing intense processing in parallel. The SEPP features a 925 MHz dual-core ARM Cortex A9 Hard Processor System (HPS), an integrated Altera Cyclone V COTS FPGA and 16 GB of flash storage.

B. NORBY Mission

NORBY is a 6U CubeSat nanosatellite (Fig. 2) by Novosibirsk State University launched on September 28, 2020 [4]. The NORBY CubeSat platform is designed to create relatively inexpensive specialised nanosatellites with a payload targeted for scientific, technological, and commercial applications. The main goals of the NORBY launch are flight tests of the platform, verification of its functional capabilities and technical solutions under real conditions in low-Earth orbit, as well as carrying out scientific and technological research envisaged by the nanosatellite payload program. The NORBY platform

connects a commercial FPGA with a LEON3 processor. The SpFi experiment was manufactured by an international cooperation between Information Satellite Systems – Reshetnev Company and Thales Alenia Space Spain.

II. SpaceFibre Technology Demonstrator

This section describes the system used for the SpFi demonstrator. Some parts are shared between both missions, and some are designed according to the specifics of each mission. The main goal of the experiments was to transmit and check as much data as possible in the timeslot in which the experiment was allowed to run.

A. SpaceFibre Demonstrator Overview

The following subsections provide an overview of the elements in the demonstrator shared between the missions. Figure 3 depicts the block diagram of the SpFi demonstrator used in both missions.

1) Software Application

While a software application is specifically designed for each mission, the goal of the software application is the same: to control and monitor the SpFi link and store the relevant results to be sent down as telemetry. The application ensures that, at the start of the experiment, the SpFi link is correctly started and configured.

Fig. 1. The OPS-SAT satellite.

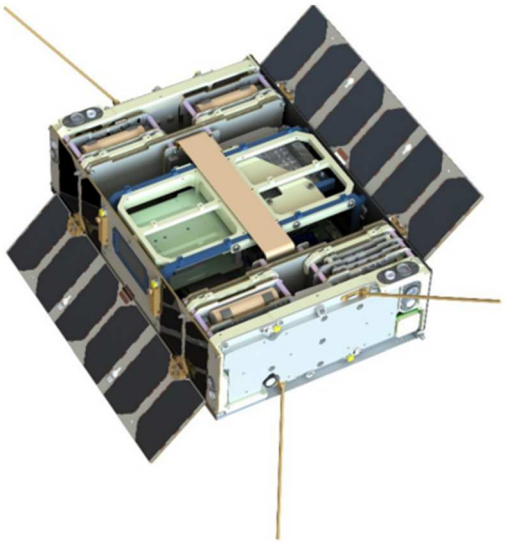

Fig. 2. The NORBY satellite.

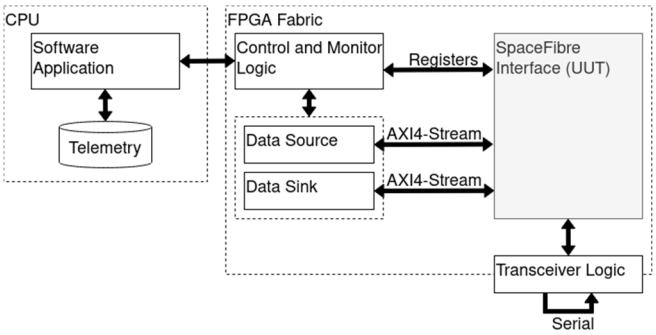

Fig. 3. SpFi demonstrator block diagram.

The low complexity of the software application is a consequence of a key feature of the SpFi protocol, which is its ease of use. SpFi just requires enabling the link and after few microseconds (typically ~40 µsec), data can be transferred at full data rate.

2) Control and Monitor Logic

This block acts as the interface between the software application and the hardware design. The information from/to the software application is stored in registers which are connected to the status and control ports of the SpFi interface, and data source/sink components.

3) Data Source and Sink

All virtual channels (VC) are connected to independent data source and data sink modules. Each transmit VC can receive data from a Source capable of providing data at the maximum rate supported by the SpFi link. This way a single VC can saturate the SpFi link with data if required. The data source generates SpFi packets. The data pattern consists of a 16-bit counter increased by 1 every transmitted data word. As the word is 32-bit wide, the value of the counter is duplicated. The counter is initialised to 0 (i.e. 0x0000) and after reaching its maximum value (i.e. 0xFFFF) it starts back from 0 again.

When the data sink detects an incorrect data pattern it reports a data error. When the sink detects an error end-of-packet (EEP), this condition is also reported. In the occurrence of an EEP or data error the data sink automatically resynchronises with the next valid word. This avoids reporting continuous false error detections whenever a packet has been truncated (EEP) or lost due to the source and the sink being out of sync.

4) Transceiver Logic

This block contains the logic to control the transceiver of the FPGA. This logic is specific to each mission to target the appropriate technology. It includes the configuration and connection of the specific clocks used by each system. Due to the SpFi experiments being adopted at a late stage on both missions, a fully representative implementation of the SpFi links was not possible. Instead, a loopback connection was used.

5) SpaceFibre Interface

This is the unit under test (UUT). It instantiates the STAR-Dundee SpFi Single-Lane Interface IP core using the configuration parameters required for each technology. For both missions the SpFi link uses two VCs to transmit and receive data at lane rate of 2.5 Gbit/s. Each SpFi VC uses an

AXI4-Stream interface to connect to the data source and sink.

B. OPS-SAT Experiment

When OPS-SAT was in its definition phase, it was not envisaged that the Altera FPGA transceivers would be required. Therefore, the transceivers pins of the FPGA were not connected to the PCB. This prevented the SpFi experiment from using the transceiver external reference clock pins, and a custom clock scheme was put in place to fix this issue.

Listed below are the main settings used in the demonstrator system for OPS-SAT:

- SpFi interface configured to use a 20-bit parallel transceiver interface.
- The interface used between the CPU and the FPGA is the Avalon Memory Mapped Interface.
- The loopback is done at the physical medium attachment (PMA).
- Included logic to also transmit, receive and check SpFi broadcast messages. The experiment transmits a broadcast message every 1 μsec.
- The software application applied a reset of the experiment every minute. The reason was to exercise more logic of the interface during the experiment and, in case of a persistent error, recover the link and continue the experiment.

C. NORBY Experiment

The NORBY mission imposed a strict constraint in the amount of telemetry space available for downloading the results of the experiment. A summary of the main parameters of the demonstrator was thus generated for download.

Listed below are the main settings used in the demonstrator for NORBY:

- SpFi interface configured to use a 32-bit transceiver interface.
- The interface used between the CPU and the FPGA is an APB interface.
- The initial approach was to perform a loopback outside the transceiver, i.e. serial loopback. Due to design limitations, the loopback was done inside the SpFi interface using its inbuilt loopback feature. This is a parallel loopback and not a serial loopback.
- The software application restarted the experiment at the beginning of each run. The duration of each run was 16 seconds.

III. Results

Both missions reached orbit successfully, and the SpFi experiments were correctly executed. This section presents the results of the experiments extracted from the telemetry received from each satellite.

A. OPS-SAT

The experiment was run in three separate campaigns with a duration of 10, 40 and 40 minutes, for a total runtime time of 90 minutes. The resulting telemetry was parsed to ensure that during each run, after the SpFi link was ready, the data generators and checkers were transmitting and receiving data at the maxim available data rate, each VC sharing almost 50% of the bandwidth. About 1% of the link bandwidth was reserved for the broadcast messages. In parallel, the link was monitored to detect anomalies in its operation, such as transient errors, but in the entire runtime no error was detected in the link.

B. NORBY

The experiment had a fixed runtime of 15.5 seconds per run. The experiment runs were launched in sets of three for a total of 92 runs. The total runtime of the experiment was around 24 minutes.

The resulting telemetry was parsed to ensure that during each run, after the SpFi link was ready, the data generators and checkers were transmitting and receiving data as expected. Due to the limits on the size of the telemetry the bandwidth utilization was extracted from the status of the VC buffers, by checking that both transmit and receive buffers reported data filling them during the experiment. In parallel, the link was monitored to detect any anomaly that could appear, such as transient errors, but in the entire runtime no error was detected in the link.

IV. Conclusion

The first publicly known missions to have tested SpaceFibre in orbit have been described. The STAR-Dundee SpaceFibre Interface IP has flown onboard OPS-SAT and NORBY. The successful results of both experiments demonstrate SpaceFibre operating in orbit. The STAR-Dundee SpaceFibre IP family [5] has been, and is currently being, implemented in FPGA and ASIC designs for several missions and products in Europe and the USA.

Acknowledgment

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