A Radiation Tolerant SpaceFibre Interface Device

SpaceWire Component, Long Paper

Steve Parkes[1], Albert Ferrer[2], Alberto Gonzalez[2], Chris McClements[2], Ran Ginosar[3], Tuvia Liran[3], Dov Alon[3], Michael Goldberg[3], Gal Sokolov[4], Gennady Burdo[4], Nimrod Blatt[4], Paul Rastetter[5], Milos Krstic[6], Alberto Crescenzio[7]

[1]*Space Technology Centre, 166 Nethergate, University of Dundee, Dundee, DD1 4EE, Scotland, UK*
[2]*STAR-Dundee, STAR House, 166 Nethergate, Dundee, DD1 4EE, Scotland, UK*
[3]*Ramon-Chips Ltd., 104 Galil Street, Nofit 36001, Israel*
[4]*ACE-IC, Caesarea, Israel*
[5]*EADS Astrium GmbH, Munich, Germany*
[6]*IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany*
[7]*Synergie CAD Instruments S.R.L., Italy*

Email: sparkes@computing.dundee.ac.uk

***Abstract*— The Very High-Speed Serial Interface (VHiSSI) device aims to provide a versatile SpaceFibre interface device in a small package. The device can act as a parallel interface device providing several modes of operation, or it can act as a SpaceWire to SpaceFibre bridge.**

This paper describes the VHiSSI chip in detail, outlines the applications it can be used for, and summarises the status of the VHiSSi project.

Index Terms*—SpaceWire, SpaceFibre, networks, spacecraft onboard processing*

I. *INTRODUCTION*

Space-based Earth observation and scientific instrumentation currently under development will push the limits of on-board data-handling technology. In the past Mil-Std 1553 and proprietary data-links were used to get instrument data from the instruments to the on-board mass memory unit and to the down-link telemetry system. Over the past decade the proprietary data links have been replaced with a standard networking technology designed for use on-board spacecraft: SpaceWire. While SpaceWire is currently being used to fulfil the on-board data-handling requirements of many missions, there are some very high data-rate instruments which are beyond its capabilities.

Several future space-based instruments, for example synthetic aperture radar (SAR) and hyper-spectral imagers, will be capable of producing data at data rates of several Gbits/s. New downlink telemetry techniques (laser and Ka-band communications) will be able to provide much higher downlink capacity than previously possible. High speed memory technologies will be able to serve multiple high data rate instruments and stream data to ground on demand. To support the growing need for onboard communications network bandwidth, technologies able to support multi-Gbits/s data transfer have been developed, e.g. Channel Link and, Wizard Link. Unfortunately these are all restricted USA devices resulting in a critical European dependency.

ESA has been developing a standard multi-Gbits/s network technology called SpaceFibre [1] [2] [3] [4]. SpaceFibre provides multi-Gbits/s data rates over fibre-optic and electrical cable. It provides a coherent quality of service mechanism able to support bandwidth reserved, scheduled and priority based qualities of service. It provides extensive fault detection, isolation and recovery (FDIR) capabilities, including a link level retry function that recovers from errors and resends data transparent to the user application. SpaceFibre uses the same packet format as SpaceWire [5] making it easy to bridge existing SpaceWire devices into a SpaceFibre network.

The VHiSSI project is a European Union Framework 7 research project which will integrate a complete SpaceFibre protocol engine, together with the physical layer interfaces, in a radiation tolerant chip manufactured by a European foundry. It will provide a complete SpaceFibre solution in a single chip.

The VHiSSI research programme aims to create very high-speed data-interface technology which is a critical component technology for future spacecraft payloads, particularly telecommunications and Earth observation payloads where multi-Gbits/s data-rates are urgently needed. A complete solution to very high-speed data networking onboard spacecraft will be provided, levering research on SpaceFibre, using a European fabrication facility, and providing a non-dependent technology.

The VHiSSI research programme will:

- Provide multi-Gbit/s serial data-link technology, essential for future spacecraft onboard data-handling systems.

- Lever prior and concurrent research on the emerging SpaceFibre standard, to provide a complete multi-Gbit/s serial technology for spacecraft onboard data-links and networks, including fault detection, isolation and recovery (FDIR) and quality of service (QoS).
- Provide a versatile chip architecture, which can be adapted and configured to support multiple applications.
- Provide the critical clock-recovery mechanism on existing European chip technology.
- Use a European semiconductor fabrication facility, enhancing and developing its capabilities for radiation tolerant chip design and production with a radiation tolerant library.
- Provide a non-dependent technology (ITAR free), allowing unrestricted use on European spacecraft and substantial export opportunities - an important capability for Europe.

This paper describes the work carried out by University of Dundee and STAR-Dundee on this project and summarises the current state of the project. The team working on this project comprises engineers from:

- University of Dundee who are leading the project, and who are responsible for project management and the VHiSSI device architecture and specification.
- Astrium GmbH who are responsible for gathering and requirements and use cases for the VHiSSI device.
- STAR-Dundee Ltd who are responsible for designing the digital part of the VHiSSI chip in register-transfer level (RTL) VHDL code.
- ACE-IC who are responsible for the design of the SerDes and CML transceivers.
- Ramon Chips who are responsible for the radiation tolerant library for the IHP chip manufacturing process and low level design of the VHiSSI device.
- IHP who are responsible for manufacturing the VHiSSI device and digital/static test of the chip.
- SCI who are responsible for supporting the high performance/analogue testing of the experimental VHiSSI chip.

II. VHiSSI Chip Architecture

The overall architectural block diagram of the VHiSSI chip is illustrated in Figure 1.

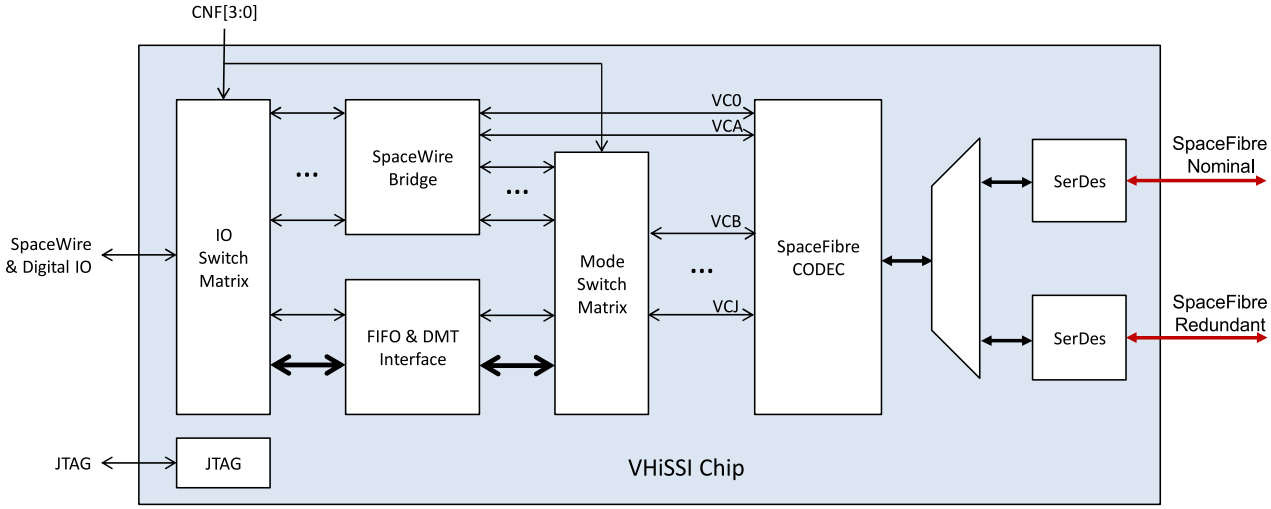

Figure 1 VHiSSI Overall Architecture

There are five main functions within the VHiSSI chip:

- SpaceWire Bridge
- FIFO, DMA, Memory and Transaction Interface
- SpaceFibre Interface
- SerDes
- IO Switch Matrix
- Mode Switch Matrix

The SpaceWire Bridge provides a bridge between SpaceWire and SpaceFibre with up to 11 SpaceWire interfaces being available. The SpaceWire Bridge includes a SpaceWire router which allows routing between SpaceWire ports and Virtual Channel (VC) buffers of the two SpaceFibre interfaces. Configuration of the VHiSSI chip can be carried out over any SpaceWire interface connected to the embedded SpaceWire router or over VC0 or VCA of the SpaceFibre interface. The

SpaceWire Bridge is connected to the IO Switch Matrix and to the Mode Switch Matrix.

The FIFO and DMA, Memory and Transaction (DMT) Interface provides various types of parallel interface into the VHiSSI chip for sending and receiving data over the SpaceFibre interfaces. The various parallel interface functions have been designed with specific application scenarios in mind and between them are able to operate with many types of local host system, including FPGAs and processors. The parallel interface is also designed to use a small number of pins, so that the VHiSSI chip can fit into a small (100 pin) package. The FIFO mode provides a direct parallel interface to two SpaceFibre virtual channels. The memory type interface provides a 32-bit bus interface for accessing VHiSSI registers or VC buffers. It is a multiplexed address/data bus, with the VHiSSI device providing an internal address latch/counter to hold the register/VC buffer address. The transaction interface is similar to the memory interface, but aims to simplify software interfacing. A single address line is used to distinguish commands and status information from data. A command is written to the VHiSSI device to specify the transaction that is about to take place. For data transfer to/from a VC buffer, a read of status information provides the status of the VC buffer identified in the command. The data transfer can then take place in a burst transfer the maximum size of which is determined by the VC buffer status information. The DMA interface puts the VHiSSI chip in control of data transfers. When there is data ready to transfer, an internal DMA controller in the VHiSSI device requests control of the external data bus. Once granted it then affects the data transfer. An external address latch/counter is required, which may be implemented in an FPGA. The FIFO and DMT interface is connected to the IO Switch Matrix and to the Mode Switch Matrix. On reset the IO pins and connections to the VC buffers from the FIFO and DMT interface and SpaceWire Bridge are determined and set by these two switch matrices.

The SpaceFibre Interface has 11 virtual channels. VC 0 is intended primarily for VHiSSI device and local system configuration and monitoring and is connected to the embedded SpaceWire router. The other VCs have programmable VC numbers and so are referred to by letters. VCA is connected to the embedded SpaceWire router. The other VCs are either connected to the SpaceWire router, directly to a SpaceWire interface, or to the parallel interface, depending on the mode of operation. Each VC supports full SpaceFibre QoS which can be configured independently for each VC. VC0 and VCA are directly connected to the embedded SpaceWire router. The other SpaceFibre VC buffers are connected to the Mode Switch Matrix which connects them to either the SpaceWire Bridge or the parallel interface. The other side of the SpaceFibre interface is connected via a multiplexer to either the nominal or redundant SerDes and CML transceiver.

The SerDes converts parallel data words from the SpaceFibre interface into a serial bit stream and vice versa. On the receive side the bit clock is recovered from the serial bit stream by the SerDes. The SerDes includes integral CML transceivers.

The IO Switch Matrix connects either the SpaceWire LVDS, SpaceWire LVTTL or parallel interface signals from the FIFO and DMT interface to the digital IO pins of the VHiSSI chip. Configuration is static and determined on exit from device reset, i.e. on the rising edge of the RSTN signal.

The Mode Switch Matrix connects either the SpaceWire Bridge or FIFO and DMT interface (parallel interface) to the VC buffers of the two SpaceFibre interfaces. Configuration is static and determined on exit from device reset, i.e. on the rising edge of the RSTN signal.

In addition to these major functions the VHiSSI chip includes a JTAG test port and some other device test modes.

III. VHiSSI Chip Applications

In this section several applications of the VHiSSI device are considered

A. High Data-Rate Instrument Interface

SpaceFibre offers substantially higher data rates than SpaceWire to support high data-rate instruments. Connection of a high data-rate instrument to a mass memory unit via SpaceFibre is illustrated in Figure 2.

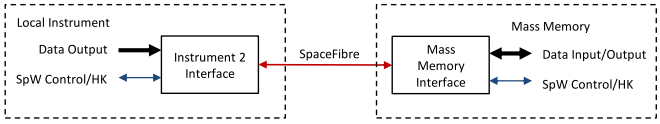

Figure 2 High Data-Rate Instrument Connected To Mass Memory

To provide data at high-speed from a local instrument to the SpaceFibre interface a parallel interface is required. To operate with current space qualified FPGAs this interface has to be 32 bits wide, which requires a 62.5 MHz interface clock (32-bits x 62.5 MHz = 2 Gbits/s, which after 8B/10B encoding is 2.5 Gbits/s signalling rate).

The simplest type of interface is a FIFO type interface, which is straightforward to connect to an FPGA. For high data rate transfer from an instrument it is only necessary to write data to an output VC buffer in the SpaceFibre interface. A slower speed interface, e.g. SpaceWire, would be useful for controlling and reading housekeeping information from the instrument.

If the instrument includes an embedded processor it may be preferable to use a memory type interface to write and read data from the SpaceFibre VC buffers in the SpaceFibre interface. This interface can then also be used to access the configuration, control and status registers inside the SpaceFibre interface. In this case it is the responsibility of the instrument to handle the transfer of data to the SpaceFibre interface.

A DMA controller included in the SpaceFibre interface transfers responsibility for data transfer from the instrument controller to the SpaceFibre interface. This may save some important processing power within the instrument controller.

The VHiSSI device is able to provide a SpaceFibre interface for high data rate instruments using a FIFO, memory or DMA type interface to an FPGA or processor. This interface is designed to be able to operate a clock speeds achievable by flight qualified FPGAs while sustaining 2 Gbits/s data transfers. It also is designed to minimise the number of pins required for the interface.

B. SpaceWire to SpaceFibre Bridge

SpaceWire has been used extensively to provide a standard interface to various instruments. To connect these instruments into a SpaceFibre based data-handling network a SpaceWire to SpaceFibre Bridge is required.

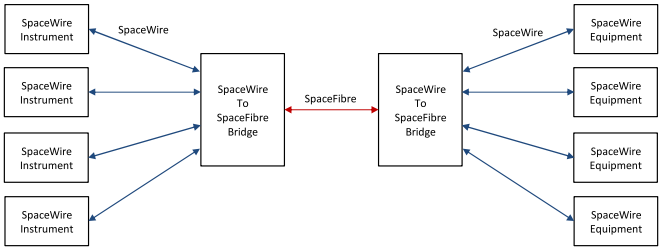

Figure 3 SpaceWire to SpaceFibre Bridge

Figure 3 shows a SpaceWire to SpaceFibre Bridge being used to multiplex several SpaceWire links over a single SpaceFibre link. In this particular example four instruments with SpaceWire interfaces are connected to some other SpaceWire enabled equipment. Bridging between SpaceWire and SpaceFibre is straightforward since both protocols use the same packet format.

The VHiSSI chip can operate as a SpaceWire to SpaceFibre bridge with either LVDS or LVTTL SpaceWire interfaces and includes an internal SpaceWire router.

C. Mass Memory Interface

A mass memory requires several SpaceFibre interface connections to support several high data-rate instruments and instruments with SpaceWire interfaces. This is illustrated in Figure 4.

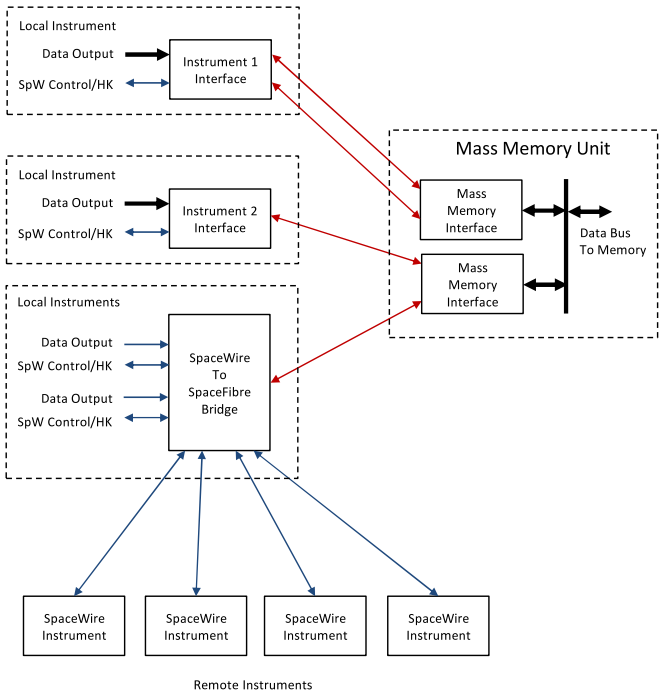

Figure 4 Mass Memory Interface

Two high data-rate instruments are shown, one with a single SpaceFibre link and the other requiring two SpaceFibre links to support data rates of 4 Gbits/s. Several SpaceWire instruments are also connected to the mass memory via a SpaceWire to SpaceFibre Bridge.

The Mass Memory unit provides four SpaceFibre interfaces connected to a common bus or network for accessing the memory modules that are to store the data.

The VHiSSI chip can provide all the SpaceFibre interfaces required in the example network of Figure 3: high-speed instrument interfaces, SpaceWire to SpaceFibre bridge and the interface to the mass memory unit.

D. Control Processor

Configuration and control information can be sent over a SpaceFibre network using individual virtual channels or a virtual network. A SpaceFibre router allows a control processor to access all the instruments and other equipment on the network as illustrated in Figure 5.

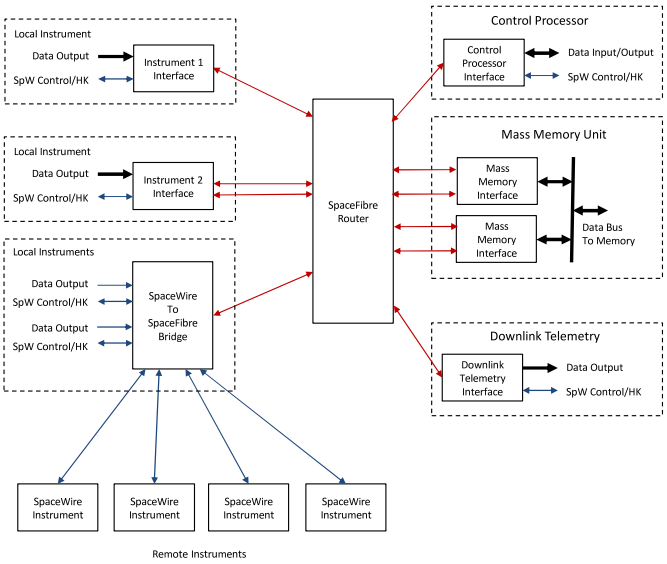

Figure 5 Control Processor on SpaceFibre Network

Figure 5 shows a complete SpaceFibre based on-board data-handling system. A SpaceFibre router is used to interconnect the various units. A control processor is connected to this router. It is able to send configuration, control and status request commands to all of the other units on the network. Typically a virtual network would be used to manage this control and status information, where one virtual channel in each unit is dedicated to control/status and each of them is given the same virtual channel number, e.g. VC0. The control processor then sends SpaceWire packets containing commands over VC0 to another unit. This unit responds over VC0. Since the control processor is the master of the VC0 virtual network, there is no undesirable contention between SpaceWire packets on VC0. This approach leaves all the other virtual channels available for data transfer.

The SpaceWire instruments do not support virtual channels, so control/status packets and data packets have to be multiplexed over the SpaceWire links. The SpaceWire to SpaceFibre Bridge must be able to support this multiplexing of SpaceWire packets containing control information, status or instrument data. This requires a SpaceWire router which could be provided within the SpaceWire to SpaceFibre Bridge. Normally configuration, control and housekeeping requests require small packets and should therefore not have a major impact on data transfer over the single SpaceWire link from instrument to the SpaceWire router in the SpaceWire to SpaceFibre Bridge.

The VHiSSI device together with a SpaceFibre router device can provide all the SpaceFibre network functionality needed for onboard data-handling architectures like that of Figure 5.

IV. Status of VHiSSI Project

A comprehensive set of requirements for the experimental VHiSSI chip have been gathered from the European spacecraft engineering community by Astrium GmbH, focusing on a small device which could be used to provide very high-speed data-links on-board a spacecraft. A versatile chip interface has been designed by University of Dundee which covers many potential applications while keeping the number of pins required on the chip to a minimum. The architectural level design of the experimental VHiSSI chip and its interface definition have been shaped, reviewed and polished and detailed design of this chip is currently underway by STAR-Dundee Ltd.

A critical part of the VHiSSI project is the radiation tolerant serialiser/deserialiser, clock-data recovery circuitry and high-speed serial driver/receiver technology. This is a demanding design activity due to the speed of the interface and the required radiation tolerance. A design has been created by ACE-IC ready for testing.

The use of the IHP chip foundry required a complete radiation tolerant component library to be designed. This has been carried out by Ramon Chips and includes logic gates, IO, LVDS IO, and memory cells. A test chip called RADIC5 has been designed and implemented which includes the critical circuitry designed by ACE-IC and library test components from Ramon Chips. This test chip is currently under test by Synergie-CAD and IHP. The results of this testing will feed into updated component design by ACE-IC and Ramon Chips which will be incorporated into the experimental VHiSSI chip.

The layout of the RADIC5 test chip is shown in Figure 6.

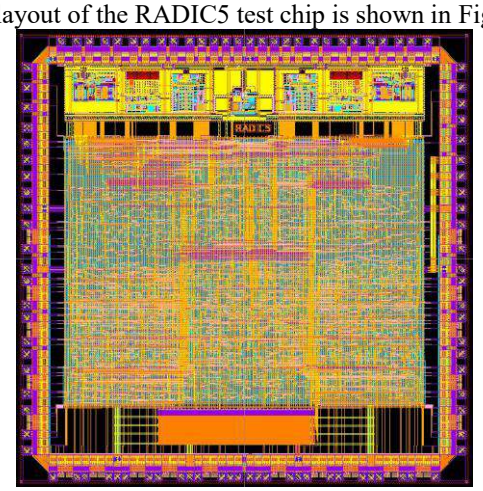

Figure 6 RADIC5 Test Chip

A radiation test board for the RADIC5 is currently being designed and will be used to support the radiation testing of the SerDes and other components on the chip.

An FPGA board is also being designed to support the functional validation and system level validation of the VHiSSI chip design prior to manufacture of the VHiSSI ASIC device. This FPGA board will also be used to provide test signals for functional testing of the VHiSSI ASIC device once it has been manufactured.

The next steps are to complete testing of the test chip, to finalise the design of the experimental VHiSSI chip, to manufacture this chip, and to test it.

V. Conclusions

SpaceFibre is a powerful, multi-Gbits/s networking technology for use on board spacecraft which has QoS and FDIR capabilities built into the hardware. The VHiSSI project is an EU Framework 7 project that is designing an experimental SpaceFibre chip. The VHiSSI chip is implemented in a small 100 pin package but provides complete SpaceFibre interface and SpaceWire to SpaceFibre bridge functionality. This chip is designed to cover the various SpaceFibre network interface requirements envisaged for different onboard systems, including SpaceWire bridging, high data-rate instrument interfacing, and mass memory unit interfacing. An initial test chip (RADIC5) has been produced to test the critical radiation tolerant SerDes technology and the radiation tolerant library components. The RADIC5 chip is currently under test. The experimental VHiSSI chip will be ready for testing during 2014.

Acknowledgment

The research leading to these results has received funding the European Space Agency under ESA contract numbers 4000102641 and from the European Union Seventh Framework Programme (FP7/2007-2013) under grant agreement n° 284389. We would also like to thank Martin Suess the ESA project manager for the SpaceFibre related activities.

References

[1] S. Parkes, A. Ferrer, A. Gonzalez, & C. McClements, "SpaceFibre Standard Draft E1", University of Dundee, 28th September 2012.

[2] S. Parkes, A. Ferrer, A. Gonzalez, & C. McClements, "SpaceFibre: Multiple Gbits/s Network Technology with QoS, FDIR and SpaceWire Packet Transfer Capabilities", International SpaceWire Conference, Gothenburg, June 2013.

[3] S. Parkes, "Never Mind the Quality, Feel the Bandwidth: Quality of Service Drivers for Future Onboard Communication Networks", paper no. IAC-10.B2.6.6, 61st International Astronautical Congress, Prague 2010.

[4] S. Parkes, C. McClements and M. Suess, "SpaceFibre", International SpaceWire Conference, St Petersburg, Russia, 2010, ISBN 978-0-9557196-2-2, pp 41-45.

[5] ECSS Standard ECSS-E-ST-50-12C, "SpaceWire, Links, Nodes, Routers and Networks", Issue 1, European Cooperation for Space Data Standardization, July 2008.