

SpaceFibre Routing Switch IP Implementation in Radiation-Tolerant FPGAs

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ABSTRACT

SpaceFibre is a technology specifically designed for use in spaceflight applications that provides point-to-point and networked interconnections at Gigabit rates with Quality of Service and Fault Detection, Isolation and Recovery. SpaceFibre is backwards compatible with SpaceWire, allowing existing SpaceWire equipment to be incorporated into a SpaceFibre network without modifications at packet level.

In this work we present the SpaceFibre Routing Switch IP Core developed by STAR-Dundee and its subsidiary STAR-Barcelona. This IP Core is fully compliant with the SpaceFibre standard – including the Network layer – thus providing a cornerstone technology necessary for future on-board data-handling systems. We also describe the capabilities and performance of the Routing Switch design. The design provides a highly flexible router comprising a number of ports and a fully configurable, non-blocking, high performance, routing switch. Finally, the implementation results of this Routing Switch IP in radiation-tolerant FPGAs are summarized and discussed. The Routing Switch IP has been carefully implemented to optimise its performance and minimise its footprint on radiation-tolerant FPGAs (e.g. RTG4, Virtex-5QV or KU060) and ASICs.

The SpaceFibre Routing Switch completes the set of essential SpaceFibre technology, providing a missing building block for the next generation of on-board data-handling systems.

1 INTRODUCTION

SpaceFibre (SpFi) is the next generation of SpaceWire (SpW) network technology for spacecraft on-board data handling. It supports high data-rate payloads, and provides robust, long distance communications for launcher applications and supports avionics applications with deterministic delivery capability. SpaceFibre provides in-built Quality of Service (QoS) and Fault Detection, Isolation and Recovery (FDIR) capabilities, and runs over electrical or fibre-optic cables. Current state-of-the-art radiation-tolerant FPGAs are perfect for SpaceFibre because they include the high-speed

Serialisers/Deserialisers (SerDes) necessary for SpaceFibre, eliminating the need for an external SerDes device. It operates at very high data rates: 3.125 Gbit/s per lane in current radiation tolerant FPGA technology and beyond 10 Gbit/s in the Kintex UltraScale KU060. Moreover, SpaceFibre has been specifically designed to be implemented efficiently and with a much smaller footprint than competing technologies.

The SpaceFibre Network layer is responsible for transferring packets over a SpaceFibre link or network. The information to be sent is packaged in the same format as SpaceWire: <Destination Address> <Cargo> <End of Packet Marker>. It uses the same routing concepts as SpaceWire including both path and logical addressing.

The SpaceFibre Routing Switch (also simply referred to as Router in this article) supports Virtual Networks (VNs) that behave like independent SpaceWire networks working at multi-gigabit rates. It also allows to bridge between SpaceWire ports and SpaceFibre Virtual Channels (VCs), providing QoS to SpaceWire networks.

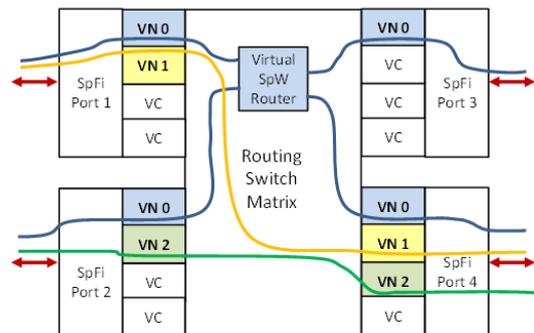


Figure 1 – Example of SpaceFibre Network

Figure 1 shows an example of how the control network and two instrument data flows are assigned to VNs in four ports of a Router. Each SpaceFibre link implements multiple VCs, each one with specific QoS parameters. For example, the bandwidth allocation parameter of each VC can be set to the expected bandwidth of each instrument, so they do not interfere with one another or with the control network. VNs are

built from the interconnection between VCs of different ports. These operate like SpaceWire networks.

2 IP CORE FEATURES

2.1 Configuration

The following characteristics can be configured in the Router IP:

- Number of ports
- Type of port interfaces
- Number of VCs for each individual SpaceFibre port

These options are defined as constants in the VHDL code. Together, they generate a highly configurable architecture, providing flexibility to the Router design to be adapted for different scenarios. This ensures that different user needs can be accommodated with ease.

2.2 Interfaces

The ports of the Router IP support SpaceFibre (with a selectable number of VCs each), SpaceWire or FIFO interfaces. Furthermore, the IP includes a configuration port that can be accessed over the RMAP protocol. The SpaceFibre operation runs up to 3.125 Gbit/s for Virtex-5QV/RTG4 and beyond 10 Gbit/s on the Kintex UltraScale 060, with guaranteed timing closure in RTG4 and Virtex-5QV with EDAC and SET filter enabled and worst-case conditions. SpaceWire can operate at link speeds of up to 200 Mbit/s for the moment (400 Mbit/s planned for the near future).

2.3 Routing Switch operation

The Router IP is fully compliant with the SpaceFibre standard including the Network layer and supports SpaceWire/SpaceFibre network capabilities such as path, logical and regional addressing. Multicast is also supported. The maximum number of VNs currently supported is 64, but each of these VNs is completely flexible: any VC of any port can be configured to any VN. The VNs can be dynamically modified using a configuration port and the RMAP protocol, via either SpaceWire or SpaceFibre. The IP Core can also be implemented in ASIC technologies.

From the performance point of view, the Router provides deterministic low latency switching. Full non-blocking switch matrix arbitration takes place when two input VCs request the same output VC. There is a packet by packet round-robin arbitration with automatic packet spill on watchdog timeout event. There are no restrictions in the connection between input and output VCs between different ports. Broadcast messages (SpaceFibre) and Time-codes (SpaceWire) are automatically broadcast to all the available ports while an internal timer locally tracks the time being distributed over the network.

The Router offers two configurable time-outs. These two timers are required to prevent the blockage of a VN in cases when the source or the sink stall in the middle of a packet, or when there is a babbling node. When timing out, the router performs automatic packet spilling of the packet causing the blockage.

3 ROUTER ARCHITECTURE

Figure 2 shows the Router high-level architecture with a configurable number of SpaceFibre and SpaceWire ports, plus the configuration port. P_x stands for port X. Each SpaceFibre port has an individually configurable number of VCs whereas the SpaceWire ports only have a single VC. The configuration port uses the RMAP protocol to configure the routing table, the VNs, the links and their corresponding QoS. The configuration port can only be accessed through VN 0. Upon reset, configuration can be performed over VC 0 of any SpaceFibre port (i.e. after reset VC 0 is mapped to VN 0).

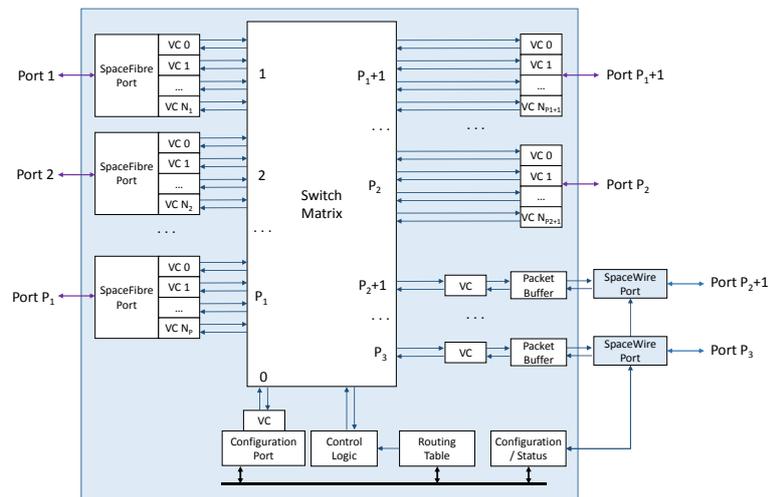


Figure 2 – SpaceFibre Router Block Diagram

The Router architecture is built around a non-blocking routing switch matrix with a number of ports. Each port can implement a number of VCs, each one comprising an input and an output VC buffer (VCB). Each VC has an associated VN number. The switch matrix interconnects one or more VCs with the same VN number, but each of these VCs must be located in a different port. The output port is selected using path or logical addressing, indicated by the leading byte of each packet and the configuration of the internal routing table. The output VCB within a port can be selected by an RMAP configuration command.

Packets belonging to different VNs never interfere with one another and do not impact the throughput and latency within the routing switch matrix. On the other

hand, when multiple packets in the same VN need to be transferred from different ports to the same output port, packet-by-packet, round-robin arbitration is performed, similarly to a SpaceWire router. This allows any combination of VNs to be implemented.

4 ROUTER IMPLEMENTATION

The SpaceFibre Router IP has been designed with existing radiation-tolerant technologies in mind. Table 1 details the synthesis resource usage of the Router IP for different configurations and FPGA technologies. Note that these values include the SpaceFibre interfaces and the additional configuration port, the routing switch matrix, all the buffers and the register space. The only block not included is the SpaceWire interface, which is very simple and thus can be neglected for this analysis. Note that the RTG4 values have been inferred. We will provide the final values in the full version of this paper. Also note that these designs do not feature TMR, but this might be desirable for the KU060. In this case for full TMR coverage the number of resources in the design will be tripled.

It is interesting to note that the resource usage increases quite linearly with the total number of VCs of the router (the configuration port and each SpaceWire or FIFO port contain a single VC). Whereas for the number of registers this can be expected, a linear increase for the total number of LUTs indicates that the architecture selected is optimal. LUT elements perform the multiplexing between input and output VCBs, and theoretically they should escalate exponentially with the number of VCs.

Ports	Virtex-5QV					
	LUT		DFF		BRAMs	
2 SpFi/2 VCs + 2 SpW	10369	13%	9188	11%	26	9%
4 SpFi/4 VCs + 4 SpW	31011	38%	24939	30%	70	23%
8 SpFi/4 VCs + 4 SpW	62217	76%	49358	60%	116	39%

Ports	RTG4					
	LUT		DFF		BRAMs	
2 SpFi/2 VCs + 2 SpW	14498	10%	10113	7%	26	12%
4 SpFi/4 VCs + 4 SpW	44682	29%	27446	18%	70	33%
8 SpFi/4 VCs + 4 SpW	96030	63%	54361	36%	116	56%

Ports	Kintex UltraScale 060					
	LUT		DFF		BRAMs	
2 SpFi/2 VCs + 2 SpW	9061	3%	9194	1%	16	1%
4 SpFi/4 VCs + 4 SpW	27926	8%	24951	4%	43	4%
8 SpFi/4 VCs + 4 SpW	60019	18%	49419	7%	71	7%
8 SpFi/8 VCs + 4 SpW	109895	33%	85424	13%	119	11%
8 SpFi/8 VCs + 8 SpFi/4 VCs + 8 SpW	227358	69%	167105	25%	189	18%

Table 1 – SpaceFibre Router Resource Usage in FPGAs

The tables show that the maximum complexity for a Router in the Virtex-5QV and RTG4 FPGAs is limited to around 40 VCs in total. These VCs can be distributed over a number of SpaceWire, SpaceFibre or FIFO ports. Therefore many ports can be implemented in these devices provided that most of the ports use few VCs. On the other hand, in the KU060 even large configurations of 70 VCs still only require around one third of the total LUT elements, and even fewer registers or memories (without TMR). Finally, a very large Router of 8 SpaceWire ports, plus 8 SpaceFibre with 8 VCs and another 8 SpaceFibre with 4 VCs (i.e. 105 VCs) has also been synthesised, showing the feasibility of such functionality inside the KU060 device.

Thanks to the flexibility offered by the Router IP, it is possible to tailor the IP for specific applications. By providing additional constraints to the number of connections possible, the design can be simplified. This can be enough for use-cases in which the VNs are known beforehand and are not susceptible to change. These can be easily mapped into a configuration HDL package. The synthesis tool will then be able to simplify and remove unused logic, optimising the resources. For example, if the VN number is always constant and equal to the VC number, the resulting Router will take less than half of the original resources.

5 IP CORE VALIDATION

The Router IP has been tested in commercial FPGAs, e.g. Xilinx Spartan and in space-grade FPGAs such as the RTG4. Figure 3 shows one of the breadboards used for the validation, a 3U PXIe board featuring a Microsemi RTG4. This board allows implementing designs with multiple SpaceFibre and SpaceWire interfaces in radiation-hardened technology. In this configuration of the board, 8 SpaceFibre and 4 SpaceWire interfaces are available. The other breadboard is very similar but uses a Xilinx Spartan-6 FPGA instead.

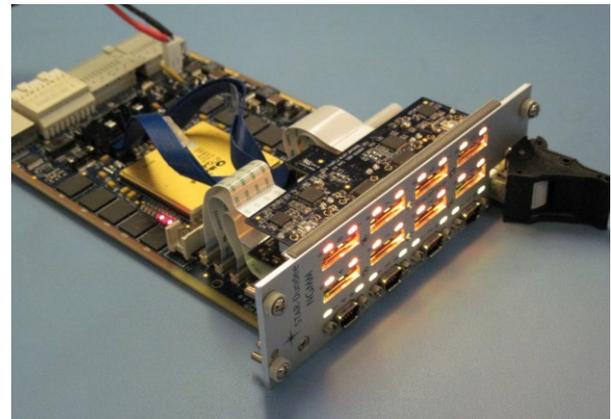


Figure 3 – SpaceFibre Router Breadboard

An activity has been promoted by ESA to perform an exhaustive validation of the Router IP and its capabilities. The validation activity "SpaceWire and SpaceFibre Network Study" carried out by Teletel, STAR-Dundee, Airbus and ISD, has recently been successfully completed. The results of this activity and the test set-up will be presented in a separate paper at this same conference, but it has confirmed that the Router operates as expected.

6 CONCLUSIONS

SpaceFibre provides multi-gigabit/s communications and incorporates a comprehensive QoS capability providing integrated bandwidth reservation, priority and scheduling. Efficient, effective and rapid FDIR mechanisms are included in the SpaceFibre interface, enabling rapid detection and recovery from link level errors.

An essential component for a SpaceFibre network is a SpaceFibre routing switch. The STAR-Dundee Routing Switch IP Core has been designed to be easy to implement in radiation-tolerant FPGAs. In this article we have detailed the performance and capabilities of the IP Core, and discussed the resources required in different radiation-tolerant FPGAs depending on several parameters such as the number and types of ports, and number of VCs.

The IP Core has been tested and subsequently validated in hardware prototypes. Both commercial and a radiation-tolerant FPGA have been used for these validation activities, ensuring full compatibility and defining an easy adoption path for this technology.

STAR-Dundee has designed and prototyped the critical SpaceFibre Router technology necessary for future on-board data-handling systems, which will lay a vital foundation for future very high data rate sensor and telecommunications systems.

7 ACKNOWLEDGMENTS

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