SpaceFibre IP Cores

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Abstract—SpaceFibre is the next generation of the widely used SpaceWire onboard network technology. It supports data rates of many Gbit/s, operates over electrical and fibre optic cables, provides quality of service (QoS) and fault detection, isolation and recovery (FDIR). This paper describes SpaceFibre interface and routing switch IP cores.

Keywords—SpaceFibre, SpaceWire, Routing Switch, Next Generation System Interconnect Standard, RTG4, SerDes, FPGA.

Introduction

SpaceFibre [1][2][3][4] is a high-reliability, high-availability, high-performance network technology for spaceflight applications. The main characteristics and capabilities of SpaceFibre are summarised below:

- Very high-performance with 3.125 Gbit/s base data rate single-lane performance in current radiation tolerant FPGAs, 10 Gbit/s base data rate with four lanes, and substantially higher data rates planned in future devices. Note that all data rates are specified including the overhead for 8B/10B encoding.
- Electrical and fibre optic media with the electrical medium supporting cable lengths up to 5 m, depending on data rate, and fibre optics supporting up to 100 m.
- High reliability and high availability using error-handling technology which is able to recover automatically from transient errors in a few microseconds without loss of information and which is able to continue operation, preserving data transfer of critical and important information, when a lane in a multi-lane link fails.
- Quality of service using multiple virtual channels across a data link, each of which is provided with a priority level, a bandwidth allocation and a schedule.
- Virtual networks that provide multiple independent traffic flows on a single physical network, which, when mapped to a virtual channel, acquire the quality of service of that virtual channel.
- Deterministic data delivery of information using the scheduled quality of service, in conjunction with priority and bandwidth allocation.
- Low-latency broadcast messages which provide time-distribution, synchronisation, event signalling, error reporting and network control capabilities.
- Small footprint which enables a complete SpaceFibre interface to be implemented in a radiation tolerant FPGA, for example, around 3% of an RTG4 FPGA for an interface with two virtual channels.
- Backwards compatibility with SpaceWire at the network level, which allows simple interconnection of existing SpaceWire [5][6] equipment to a SpaceFibre link or network.

This paper first describes a typical SpaceFibre network. It then outlines the main characteristics of the single-lane and multi-lane SpaceFibre interface IP cores. The SpaceFibre routing switch IP core is then introduced.

SpaceFibre Networks

SpaceFibre can be used to provide high data-rate point-to-point links between instruments and mass-memory. It can also be used to form a complete data-handling network using a SpaceFibre routing switch to interconnect instruments, mass-memory, downlink transmitter, payload processors, data compressors and control computers. Such a spacecraft onboard network is shown in Figure 1 [7].

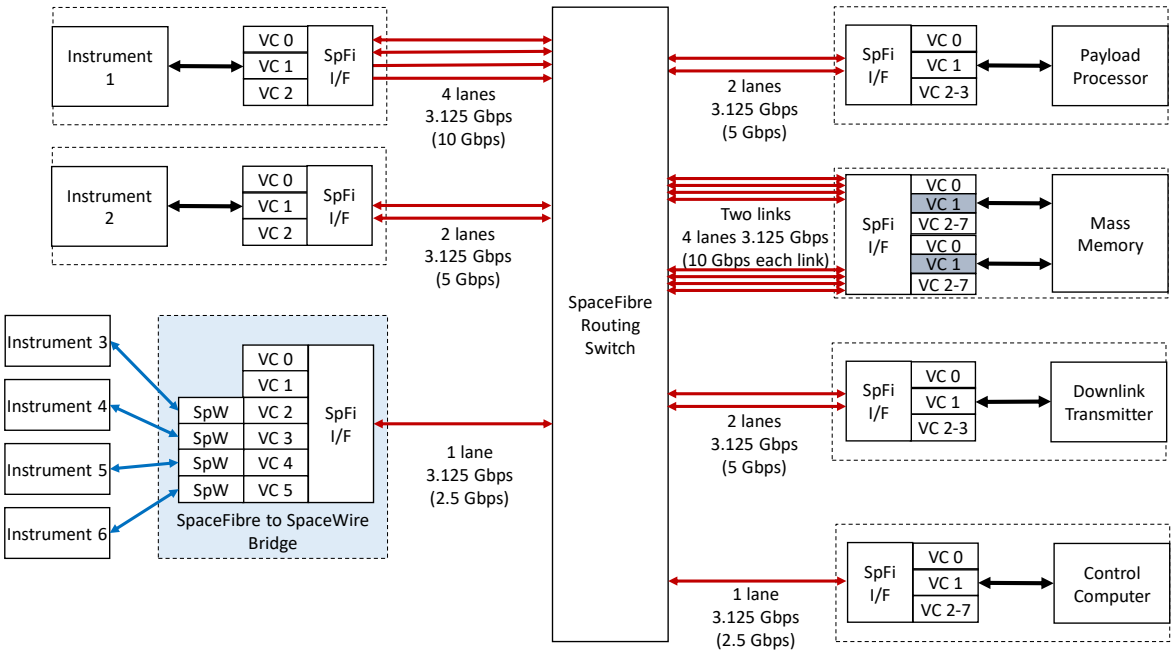

Figure 1: Example SpaceFibre Payload Data-Handling Network

The SpaceFibre routing switch has eight ports, with various numbers of lanes. All lanes throughout the network operate at 3.125 Gbit/s. There are two high data-rate instruments; Instrument 1 which requires four lanes and Instrument 2 which requires two lanes. Each of these instruments has three virtual channels with VC0 being used for network control, VC1 for instrument control and VC2 for instrument data. The SpaceFibre routing switch maps the virtual channels to virtual networks, so that, for example, Instrument 1 VC 2 is mapped to virtual network 2 (VN2) and Instrument 2 VC2 is mapped to VN3.

There are four instruments with SpaceWire interfaces that are connected to a SpaceWire to SpaceFibre bridge.

The mass-memory unit has two SpaceFibre interfaces with four lanes each. Together they provide a data rate of up to 20 Gbit/s into the mass memory unit. The downlink transmitter has a dual-lane SpaceFibre interface supporting data rates of up to 5 Gbit/s. A payload data processing system is also included in the network again with two virtual channels used for data transfer.

A control computer is connected to the network using a single-lane SpaceFibre interface. It provides both network management and equipment management services. Network management commands and responses travel over VC0 mapped to VN0, and equipment management commands and responses travel over VC1 mapped to VN1. Through the SpaceFibre network the control computer is able to configure control and monitor all the equipment attached to the network.

SpaceFibre Interface IP Core

The single-lane SpaceFibre IP core has four principal types of interface, as shown in Figure 2:

- The virtual channel interfaces, one for each virtual channel, which each provide an interface for sending packets over the virtual channel and an interface for receiving packets.
- The broadcast interface, which is used to send broadcast messages, which are broadcast to all the units on the network.
- The management interface, which is used to configure, control and monitor the SpaceFibre interface.
- The SerDes interface, which is used to connect the IP core to the serialiser-deserialiser. If the SerDes does not include the 8B/10B encoder/decoder the IP core can be configured to provide these functions.

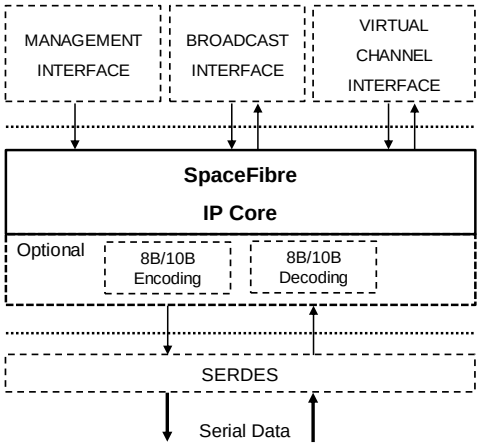

Figure 2: SpaceFibre Single-Lane IP Core Interfaces

The SpaceFibre Single-Lane IP core includes the following features:

- Compliant with the SpaceFibre standard.
- Support lane rates up to 3.125 Gbit/s in an RTG4 or Virtex-5QV FPGA.
- Guaranteed timing closure in RTG4 or Virtex-5QV with EDAC and SET filter enabled and worst-case conditions.
- Highly configurable, giving flexibility through generics in the VHDL source. The following characteristics can be configured:
    - Addition of inbuilt 8B/10B encoder/decoder
    - Number of Virtual Channels
    - Size of the Virtual Channel buffers
- Simple data interfaces based on standard input and output FIFO interfaces (32-bit AXI4-Stream).
- Independent user-defined data read and write AXI clocks.
- Automatically recovers from transient errors in less than 4 µs without loss of data.
- Ability to start one end of the link in a low-power mode while waiting for the other end to become active.
- Optimised for low latency operation, including 80-bit broadcast interface for ultra-low latency short messages (< 400 ns).
- Validated in major FPGA families including radiation hard devices, e.g. Microsemi RTG4 and RTAX, and Xilinx Virtex-5QV.

The RTG4/Virtex-5QV resources required by the SpaceFibre module including transmit and receive FIFOs are detailed below for different Virtual Channels.

Table 1: FPGA Resources Required for SpaceFibre Single-Lane IP Core

	RTG4 [1]			**Virtex-5QV**		
	LUT	**DFF**	**RAM Block** [2]	**LUT**	**DFF**	**RAM Block**
1 VC	3944 2.6%	2818 1.9%	4 1.9%	2750 3.4%	2365 2.9%	4 1.3%
2 VC	4454 2.9%	3197 2.1%	6 2.9%	3138 3.8%	2596 3.2%	6 2.0%

[1] 8B/10B encoding performed inside the IP Core

[2] Only RAM1K18 blocks are used. No RAM64x18 blocks are required

SpaceFibre Multi-Lane IP

Multi-lane operation is an optional capability of the SpaceFibre interface which increases the data throughput compared to a single-lane link and also provides graceful degradation and/or redundancy in the event of a lane failing. Two or more lanes operate together as a single link. Because the logic to initialise a lane and monitor its status is located below the Multi-Lane layer, the lanes can be initialised and operated independently of each other. This feature enables automatic graceful degradation, spreading traffic over the remaining working lanes automatically in the event of a lane failure.

Single-lane SpaceFibre implementations must be bidirectional even if the end-user data flow is unidirectional, because of the feedback required by the protocol. However, in a multi-lane implementation only one bidirectional lane is enough for protocol related information. Other lanes can be unidirectional, saving power and mass. This is illustrated in Figure 3.

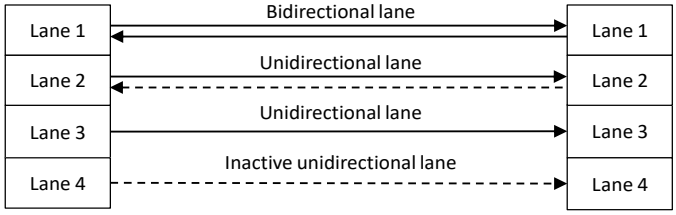

Figure 3: SpaceFibre Bidirectional, Unidirectional and Inactive Lanes in a Multi-Lane Link

In this quad-lane configuration example, bidirectional lane 2 can be set to a unidirectional lane for power saving reasons. Unidirectional Lane 4 can be enabled when one lane fails, or when a higher data rate is required. It is also possible to send data using all four lanes and add an additional one configured as a hot redundant lane, which only sends data when another lane fails.

The multi-lane IP core adds the following features to those of the single-lane IP core.

- Configurable number of independent lanes (up to maximum of 16) with cold and hot redundancy.
- Automatic graceful degradation when a lane fails.
- Hot redundant lanes recover from lane failures in less than 2 µs without user intervention.
- Lanes can be configured as unidirectional to save power and mass in asymmetric data flows.
- Wide AXI4-Stream interface to support slow user clock.
- Lane rates up to 3.125 Gbit/s in RTG4 or Virtex-5QV are supported (e.g. aggregate rates of up to 6.25 Gbit/s using 2 lanes or up to 12.5 Gbit/s using 4 lanes).
- Guaranteed timing closure with EDAC and SET filter enabled and worst-case conditions.

The resources required by a SpaceFibre design in RTG4/Virtex-5QV including transmit and receive FIFOs are detailed below for different number of lanes and Virtual Channels.

Table 2: FPGA Resources Required for SpaceFibre Multi-Lane IP Core

	RTG4 [1]			**Virtex-5QV**		
	LUT	**DFF**	**RAM Block** [2]	**LUT**	**DFF**	**RAM Block**
2 Lanes 1 VC	6494 4.3%	5351 3.5%	8 3.8%	3858 4.7%	3938 4.8%	8 2.7%
2 Lanes 2 VC	7314 4.8%	6088 4.0%	12 5.7%	4503 5.5%	4382 5.3%	12 4.0%
3 Lanes 2 VC	8997 5.9%	7413 4.8%	12 5.7%	5416 6.6%	5226 6.4%	12 4.0%

[1] 8B/10B encoding performed inside the IP Core

[2] Only RAM1K18 blocks are used. No RAM64x18 blocks are required

SpaceFibre Routing Switch IP Core

The STAR-Dundee SpaceFibre Router IP Core provides a highly flexible SpaceFibre router comprising a number of SpaceFibre interfaces and a fully configurable, non-blocking, hig- performance, routing switch.

The SpaceFibre router supports an arbitrary number of virtual networks that behave like independent SpaceWire networks working at multi-gigabit rates. The virtual networks can be set statically through FPGA programming or can be dynamically modified using the configuration port and the RMAP protocol, via SpaceFibre.

The IP Core has been optimised to work with high-performance radiation-tolerant FPGAs using up to eight virtual channels per port, each with its own quality of service parameters. The IP Core can also be implemented in radiation-tolerant ASIC technologies.

Conclusion

The full paper will provide further information about the SpaceFibre Routing Switch IP Core.

Acknowledgment

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