

# Testing SpaceFibre Interfaces and Systems

Steve Parkes<sup>(1)</sup>, David Gibson<sup>(1)</sup>, Stephen Mudie<sup>(1)</sup>, Chris McClements<sup>(1)</sup>,

<sup>(1)</sup> STAR-Dundee Ltd, Star House, 166 Nethergate, Dundee, DD1 4EE, Scotland, UK.

Email: [steve.parkes@star-dundee.com](mailto:steve.parkes@star-dundee.com); [david.gibson@star-dundee.com](mailto:david.gibson@star-dundee.com);

[stephen.mudie@star-dundee.com](mailto:stephen.mudie@star-dundee.com); [chris.mcclements@star-dundee.com](mailto:chris.mcclements@star-dundee.com);

Albert Ferrer Florit<sup>(2)</sup>, Alberto Gonzalez Villafranca<sup>(2)</sup>

<sup>(2)</sup> STAR-Barcelona S.L., Av. Cerdanyola, 79-81, Planta 2, Oficina 2, 08172 Sant Cugat del Vallès, Barcelona, Spain.

Email: [albert.ferrer@star-dundee.com](mailto:albert.ferrer@star-dundee.com); [albert.gonzalez@star-dundee.com](mailto:albert.gonzalez@star-dundee.com);

## ABSTRACT

SpaceFibre is a very high performance, high reliability and high availability network for spaceflight applications. Test equipment is necessary which can operate at many Gbit/s, and which can present the various layers of SpaceFibre in an intuitive manner to support equipment debugging and system integration. This paper will describe the latest test equipment designed by STAR-Dundee for SpaceFibre and how it can be used to accelerate development of next generation payload processing systems.

## 1 INTRODUCTION

SpaceFibre [1-4] is a new generation of SpaceWire [5-6] technology which provides the high data rates required by Earth observation and communications payloads. It delivers robust, long distance communications for launcher applications and supports avionics applications with deterministic delivery constraints. SpaceFibre enables a common on-board network to be used across many different mission applications resulting in cost reduction and design reusability [7].

The key features of SpaceFibre are outlined below [8]:

- Very high-performance, with 3.125 Gbit/s single-lane performance (including overhead for 8B/10B encoding) in the Microsemi RTG4, giving 12.5 Gbit/s with four lanes, and 6.25 Gbit/s per lane in Xilinx XQRKU060 and Microchip PolarFire, giving 25 Gbit/s with four lanes.
- Electrical and Fibre Optic media with the electrical medium supporting cable lengths up to 5 m, depending on data rate, and fibre optics supporting up to 100 m.
- High reliability and high availability using error-handling technology which is able to recover automatically from transient errors in a few microseconds without loss of information and which is able to continue operation, preserving transfer of critical and important information when a lane in a multi-lane link fails.
- Multi-lane capability providing increased bandwidth aggregated into an overall link

bandwidth, rapid (few  $\mu$ s) graceful degradation in the event of a lane failure, hot and cold lane redundancy, and support for asymmetric traffic with unidirectional lanes.

- Quality of service using multiple virtual channels across a data link, each of which is provided with a priority level, a bandwidth allocation and a schedule.
- Virtual networks that provide multiple independent traffic flows on a single physical network, which, when mapped to a virtual channel, acquire the quality of service of that virtual channel.
- Deterministic data delivery of information using the scheduled quality of service, in conjunction with priority and bandwidth allocation.
- Low-latency broadcast messages which provide time-distribution, synchronisation, event signalling, error reporting and network control capabilities.
- Small footprint which enables a complete SpaceFibre interface to be implemented in a radiation tolerant FPGA, for example, around 3% of an RTG4 FPGA for a typical instrument interface with two virtual channels.
- Backwards compatibility with SpaceWire at the network level, which allows simple interconnection of existing SpaceWire equipment to a SpaceFibre link or network.

With such a rich set of features appropriate, high-performance test equipment is necessary which can present the various layers of SpaceFibre in an intuitive manner to support equipment debugging and system integration. This paper briefly describes the widely used STAR Fire test equipment for SpaceFibre. The latest test equipment for SpaceFibre is then described covering its performance and capabilities in some detail.

## 2 STAR FIRE

The STAR Fire was an essential work horse during the design and development of the SpaceFibre standard and was widely used by early adopters of SpaceFibre.

The STAR Fire Mk3 is an evolution of the initial STAR Fire device [9]. It has two SpaceFibre and two SpaceWire interfaces, two Mictor connectors for connecting a Logic Analyser, and four SMB connectors. Three of those are external input triggers, and one is an external output trigger. A block diagram of the STAR Fire Mk3 is shown in Figure 1 along with a photograph in Figure 2.

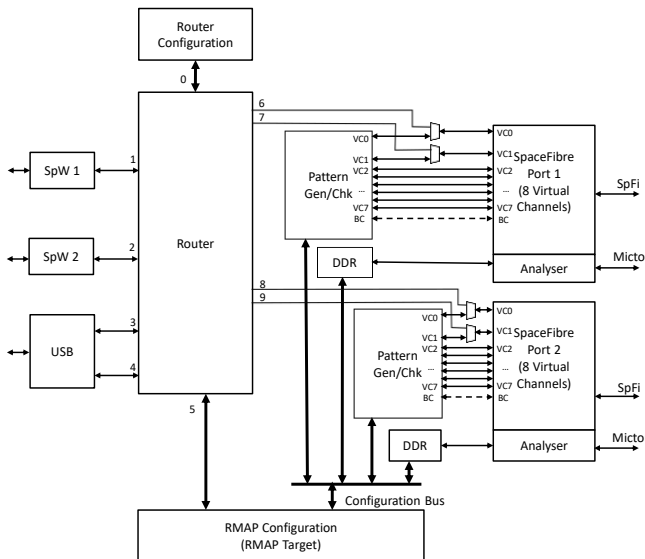


Figure 1: STAR Fire Mk3 architecture

The STAR Fire Mk3 can operate as a SpaceFibre link analyser, SpaceFibre interface and as a bridge between SpaceFibre and SpaceWire. It has embedded pattern data generators and checkers for high data-rate packet generation and checking. The Mk3 has a USB 3.0 interface, which provides high data-rate communications with a host PC.



Figure 2: STAR Fire Mk3 unit

The STAR Fire Mk3 is also able to operate as a SpaceFibre Link Analyser. It can transparently capture SpaceFibre traffic on a single link in both directions and is able to trigger the data capture upon detection of SpaceFibre words, symbol patterns or errors.

To display the captured SpaceFibre traffic, four independent views are provided:

- Symbol view which shows the symbols being sent over the link and the words that these symbols make up.
- Frame view which shows the frames from the virtual channels being multiplexed over the single physical link.
- Packet view which shows the packet data being sent over each virtual channel.
- Network view which provides a means of rapidly navigating through the large amount of captured data.

When a SpaceFibre traffic item is selected in one view, each of the other views automatically navigate to their corresponding item.

The STAR Fire Mk3 is not able to operate with a link speed of more than 3.125 Gbit/s, does not support multi-lane operation and has a limited bandwidth to the host computer of around 1.8 Gbit/s. There is a need for test equipment which is able to overcome these performance limitations and to enhance the usability of the equipment.

### 3 STAR-ULTRA PCIE

The STAR-Ultra PCIe was developed to overcome the limitations of the STAR Fire Mk3 and to provide efficient and effective test equipment for SpaceFibre in support of equipment development, ASIC design and network integration.

The STAR-Ultra PCIe is an 8-lane PCIe Gen 3 board with two quad-lane interfaces. It has two quad-lane SpaceFibre interfaces.

The STAR-Ultra PCIe has three main functions:

- Sending data from a host PC to an element under test over SpaceFibre at up to 10 Gbit/s
- Receiving data from an element under test to a host PC over SpaceFibre at up to 10 Gbit/s
- Capturing and analysing data travelling over SpaceFibre to support element and system-level debugging

The performance of the STAR-Ultra PCIe is as follows:

- Maximum data rate per lane 6.25 Gbit/s
- Maximum data rate per link over 10 Gbit/s
- Maximum data rate to host PC over 10 Gbit/s

A photograph of the STAR-Ultra PCIe is shown in Figure 3. The board is inserted in a host computer with a QSFP to 4xSFP cable in the board. A STAR-Dundee SPF to SMP adaptor is also shown in this photograph. This arrangement allows the STAR-Ultra PCIe to be used with a wide range of connectors on the unit under test, including the following:

- QSFP (SpFi-TypeD-QSFP)
- SFP (SpFi-TypeD-SFP/SPF+) using QSFP to SFP+ cable
- SMP (SpFi-TypeD-SMP)
- SMA (SpFi-TypeD-SMA) using SMP to SMA cables
- SMPM (SpFi-TypeD-SMPM) using SMP to SMPM cables

Another adaptor is available for SpaceFibre TypeC (eSATA) connectors. Some other adaptors are also under development.



**Figure 3: STAR-Ultra in a PC with an SMP Adaptor**

The STAR-System software that comes with the STAR-Ultra PCIe includes:

- High-performance software drivers
- SpaceFibre configuration and control software
- User data transmit and receive applications
- Link analyser control and display software

The SpaceFibre link analyser software provides clear visibility of the various protocol layers of SpaceFibre and enables rapid inspection of large volumes of data. Figure 4 to Figure 8, which are appended to the end of this paper, illustrate the capabilities of the link analyser.

Figure 4 shows a screenshot of the word view. This view shows the individual symbols and words that are used to initialise and send data over a SpaceFibre link and to recover communications after a failure. The link being analysed is a four-lane link and each of the lanes have their own column. On the left-hand side of the display is shown the activity in one direction and on the right-hand the activity in the other direction. Time increases down the screen. It is possible to scroll up and down and to

search for specific symbols and words. This view is particularly helpful when debugging the low-level of SpaceFibre.

Figure 5 shows a combined frame and word view. The frame view shows each virtual channel in a separate column and the frames that are flowing over the link. Frames are multiplexed over the link to provide the separate virtual channels and to support the quality of service of the virtual channels. This figure also shows that the various analyser views can be shown concurrently and are automatically synchronised, with all views being centred around the same point in the traffic flowing over the link. There is also a packet view which shows the packet data flowing over each of the virtual channels. The packet data can be shown in various formats.

Figure 6 shows the network or navigation view. This view is used to navigate around the large amount of data that can be captured by the link analyser. Time progresses from left to right and each virtual channel is shown as a series of rows. Each trace shows the volume of user data that is flowing over the link over each of the virtual channels. VC1 is not sending any data initially and then around 500µs on the timeline at the top, it starts to send packets. The display is zoomed out, so it is not possible to see the individual packet that are being used to transfer the user data over a virtual channel. It is possible to grab the grey bar on the top left and move it to the right to look at more data. The size of the green bar at the top shows the proportion of the complete data capture that is being shown. Here the green line takes up most of the display width showing that about 80% of the data stored is being viewed. Using the mouse or touch pad it is possible to zoom into the data.

Figure 7 shows what happens as the user zooms into the data. As can be seen by the green line at the top, about 10% of the data is being shown. The two vertical black lines are the click and drag zoom region that is being selected. Dynamically the display changes to showing the frames and packets, in dark blue, as well as the grey data volume line. It is now possible to see that each of the dips in the traffic volume corresponds to the virtual channel stopping sending frames.

Figure 8 shows the result of zooming in even further. Now each of the individual frames are clearly visible (the dark blue blocks) and the multiplexing of those frames from the different virtual channels is apparent. The pink lines in the frames show the end of packet markers. The green line at the top shows that around 1% of the data captured is being displayed in the detailed view. As the user scrolls to the left or right or picks a point to look at using the cursor, the display will centre on that point and the word, frame and packet views will all focus on that point. This provides a simple and intuitive, but powerful means of scanning through vast

amounts of data looking for potential anomalies and then instantly being able to see the full detail.

#### 4 CONCLUSIONS

SpaceFibre provides a high-performance, high-reliability and high-availability network technology specifically designed for spaceflight applications. It is simple to provide network interfaces to instruments, data storage units, data compressors, other forms of data processor, downlink transmitters and to the control computer. The latest SpaceFibre test equipment from STAR-Dundee provides the performance and capabilities required for the design, development, unit test and integration of the next generation of spacecraft payload data-handling equipment benefitting from SpaceFibre technology.

#### 5 ACKNOWLEDGMENTS

The research leading to these results has been supported in part with funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 776151.

#### 6 REFERENCES

- [1] ECSS Standard ECSS-E-ST-50-11C, "SpaceFibre – Very high-speed serial link", European Cooperation for Space Data Standardization, 15<sup>th</sup> May 2020. Available from <http://www.ecss.nl>.
- [2] S. Parkes, C. McClements and M. Suess, "SpaceFibre", International SpaceWire Conference, St Petersburg, Russia, 2010, ISBN 978-0-9557196-2-2, pp 41-45.
- [3] S. Parkes et al, "SpaceFibre: Multi-Gigabps Interconnect for Spacecraft On-board Data Handling", IEEE Aerospace Conference, Big Sky, Montana, 2015.
- [4] A. Ferrer Florit, A. Gonzalez Villafranca and S. Parkes, "SpaceFibre Multi-Lane", International SpaceWire Conference, Yokohama, Japan, 2016, ISBN 978-0-9954530-0-5.
- [5] ECSS Standard ECSS-E-ST-50-12C, "SpaceWire, Links, Nodes, Routers and Networks", Issue 1, European Cooperation for Space Data Standardization, July 2008, available from <http://www.ecss.nl>.
- [6] S. Parkes, "SpaceWire Users Guide", ISBN: 978-0-9573408-0-0, STAR-Dundee, 2012, available from <https://www.star-dundee.com/knowledge-base/spacewire-users-guide> (last visited 11th Feb 2018).
- [7] Albert Ferrer Florit, Alberto Gonzalez Villafranca, Marti Farras Casas and Steve Parkes, "SpaceFibre Routing Switch IP Implementation in Radiation-Tolerant FPGAs", DASIA 2019.
- [8] S.Parkes, Albert Ferrer Florit and Alberto Gonzalez Villafranca, "SpaceFibre Interfaces and Architectures" IEEE Aerospace, Big Sky, Montana, USA, March 2019.

	Lane 0	Lane 1	Lane 2	Lane 3	-- Tx 1 Rx 1 --	Lane 0	Lane 1	Lane 2	Lane 3
74.5088 μs	INIT1	INIT1	INIT1	INIT1		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
74.5216 μs	REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES		REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES
74.528 μs	INIT1	INIT1	INIT1	INIT1		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
74.5344 μs	INIT1	INIT1	INIT1	INIT1		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
81.1072 μs	REPEATED 1027 TIMES	REPEATED 1027 TIMES	REPEATED 1027 TIMES	REPEATED 1027 TIMES		REPEATED 1027 TIMES	REPEATED 1027 TIMES	REPEATED 1027 TIMES	REPEATED 1027 TIMES
81.1136 μs	INIT2	INIT2	INIT2	INIT2		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
83.328 μs	REPEATED 346 TIMES	REPEATED 346 TIMES	REPEATED 346 TIMES	REPEATED 346 TIMES		REPEATED 346 TIMES	REPEATED 346 TIMES	REPEATED 346 TIMES	REPEATED 346 TIMES
83.3344 μs	INIT2	INIT2	INIT2	INIT2		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
83.3408 μs	INIT2	INIT2	INIT2	INIT2		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
83.36 μs	REPEATED 3 TIMES	REPEATED 3 TIMES	REPEATED 3 TIMES	REPEATED 3 TIMES		REPEATED 3 TIMES	REPEATED 3 TIMES	REPEATED 3 TIMES	REPEATED 3 TIMES
83.3664 μs	INIT2	INIT2	INIT2	INIT2		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
83.3728 μs	INIT3 (LR 1, LS 1, DS 0)	INIT3 (LR 1, LS 1, DS 0)	INIT3 (LR 1, LS 1, DS 0)	INIT3 (LR 1, LS 1, DS 0)		INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)
83.3792 μs	INIT3 (LR 1, LS 1, DS 0)	INIT3 (LR 1, LS 1, DS 0)	INIT3 (LR 1, LS 1, DS 0)	INIT3 (LR 1, LS 1, DS 0)		INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)
83.3984 μs	REPEATED 3 TIMES	REPEATED 3 TIMES	REPEATED 3 TIMES	REPEATED 3 TIMES		REPEATED 3 TIMES	REPEATED 3 TIMES	REPEATED 3 TIMES	REPEATED 3 TIMES
83.4048 μs	IDLE	IDLE	INIT3 (LR 1, LS 1, DS 0)	IDLE		INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)
83.4112 μs	IDLE	IDLE	IDLE	IDLE		INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)
83.4176 μs	IDLE	IDLE	IDLE	IDLE		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
83.424 μs	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
83.4304 μs	REPEATED 1 TIME	REPEATED 1 TIME	REPEATED 1 TIME	REPEATED 1 TIME		REPEATED 1 TIME	REPEATED 1 TIME	REPEATED 1 TIME	REPEATED 1 TIME
83.4368 μs	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
83.4432 μs	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
83.4496 μs	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
83.456 μs	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
83.4624 μs	REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES		REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES
83.4752 μs	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)		UNKNOWN	UNKNOWN	UNKNOWN	UNKNOWN
83.4816 μs	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)		INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)	INIT3 (LR 1, LS 0, DS 0)
83.488 μs	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)		FRBS	FRBS	FRBS	FRBS
83.4944 μs	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)		FRBS	FRBS	FRBS	FRBS
83.5008 μs	REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES		REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES
83.5328 μs	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)		FRBS	FRBS	FRBS	FRBS
83.5392 μs	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)		FRBS	FRBS	FRBS	FRBS
83.5456 μs	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)		FRBS	FRBS	FRBS	FRBS
83.584 μs	REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES		REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES
83.5904 μs	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)		FRBS	FRBS	FRBS	FRBS
83.5968 μs	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)		FRBS	FRBS	FRBS	FRBS
83.6352 μs	REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES		REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES
83.6416 μs	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)	ALIGN (LANE COUNT 4, L 1..3)		FRBS	FRBS	FRBS	FRBS
83.648 μs	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)	ACTIVE (ACTIVE LANES 0..3)		FRBS	FRBS	FRBS	FRBS
83.6544 μs	REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES		REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES	REPEATED 6 TIMES

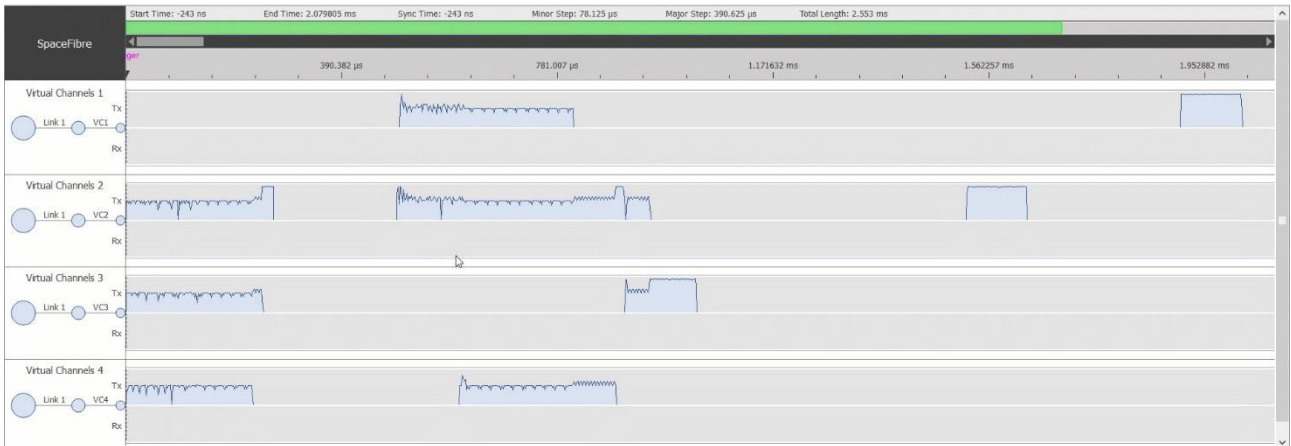
Figure 4: STAR-Ultra PCIe Used for Debugging SpaceFibre Link Initialisation

	VC1	VC2	VC3	VC4
205.126 μs			SDP (254 wcr..)	
205.407 μs			EOP	SDP (254 wcr..)
205.446 μs				
205.523 μs			SDP (Seq +01)	
205.561 μs				
205.567 μs			SDP (254 wcr..)	
205.836 μs				SDP (Seq +0)
205.843 μs				SDP (254 wcr..)
205.939 μs			EOP	
205.964 μs				
205.996 μs			SDP (Seq +23)	EOP
206.003 μs				
206.278 μs				SDP (Seq +11)
206.291 μs			SDP (Seq +23)	

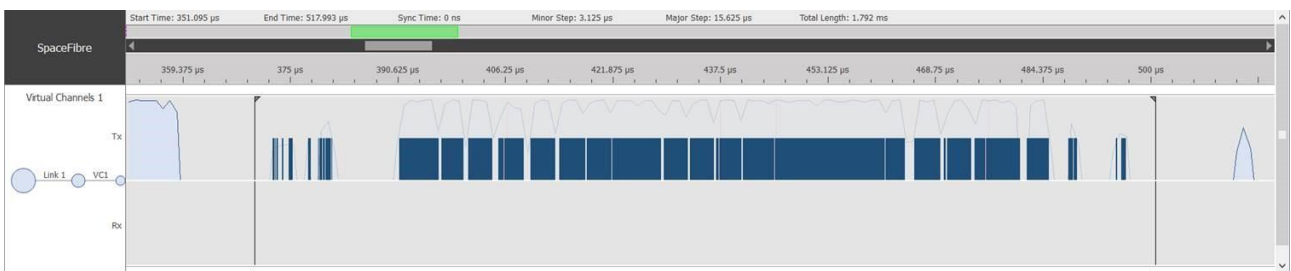
  

	Word 0	Word 1	Word 2	Word 3	-- Tx 1 Rx 1 --	Word 0	Word 1	Word 2	Word 3
205.6832 μs	REPEATED 14 TIMES	REPEATED 14 TIMES	REPEATED 14 TIMES	REPEATED 14 TIMES		REPEATED 14 TIMES	REPEATED 14 TIMES	REPEATED 14 TIMES	REPEATED 14 TIMES
205.6896 μs	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)		ACK (SEQ +20, CRC 0a24)			
205.696 μs	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)		DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)
205.728 μs	REPEATED 5 TIMES	REPEATED 5 TIMES	REPEATED 5 TIMES	REPEATED 5 TIMES		REPEATED 5 TIMES	REPEATED 5 TIMES	REPEATED 5 TIMES	REPEATED 5 TIMES
205.7344 μs	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)		SDP (SEQ +0, CRC 0aFES..)			
205.7408 μs	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)		SDP (VC 3)			
205.7472 μs	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)		DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)
205.856 μs	REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES		REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES
205.8624 μs	ACK (SEQ +0, CRC 0a08)					DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)
205.8688 μs	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)		DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)
205.9264 μs	REPEATED 9 TIMES	REPEATED 9 TIMES	REPEATED 9 TIMES	REPEATED 9 TIMES		REPEATED 9 TIMES	REPEATED 9 TIMES	REPEATED 9 TIMES	REPEATED 9 TIMES
205.9328 μs	DATA (0a5E, EOP)	DATA (F11a)	DATA (F11a)	DATA (F11a)		DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)
205.9392 μs	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)		DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)
205.9456 μs	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)		DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)
205.952 μs	PCI (MULTI 2, VC 2, SEQ..)					DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)
205.9584 μs	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)		DATA (0a35555555)	DATA (F11a)	DATA (F11a)	DATA (F11a)
205.9648 μs	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)		DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)
205.9776 μs	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)		DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)
205.9904 μs	REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES		REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES	REPEATED 2 TIMES
205.9968 μs	SDP (SEQ +21, CRC 0a00..)					DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)
206.0032 μs	SDP (Seq +3)					DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)	DATA (0a35555555)

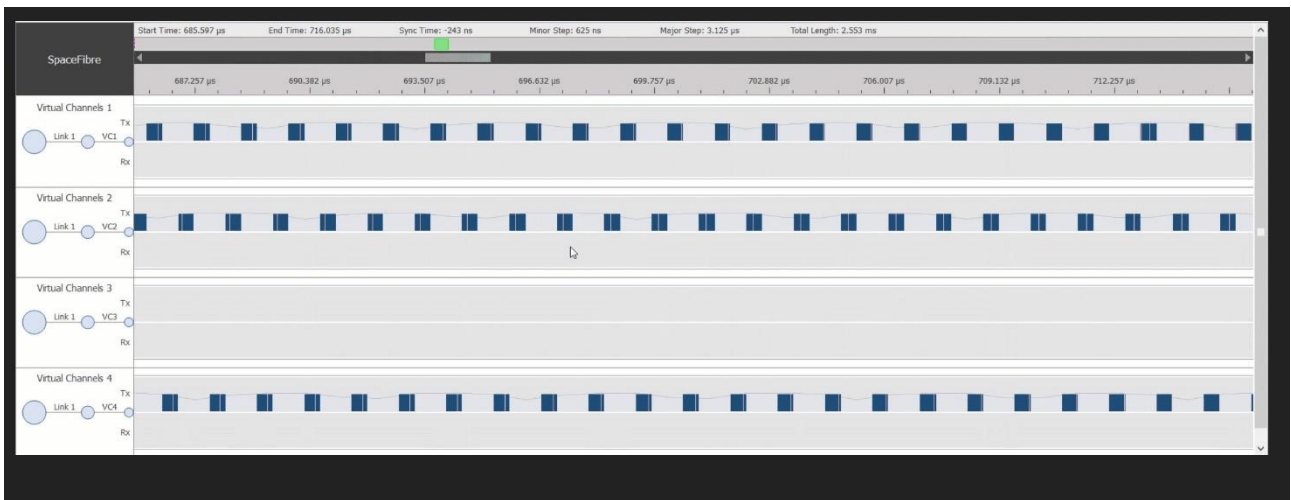
Figure 5: STAR-Ultra PCIe Frame and Word view



**Figure 6: STAR-Ultra PCIe Link Analyser Network Summary View**



**Figure 7: STAR-Ultra PCIe Link Analyser Network Summary View and Detailed View**



**Figure 8: STAR-Ultra PCIe Link Analyser Network Detailed View**