SpaceFibre – An Update

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ABSTRACT

The SpaceFibre standard was published in May 2019 and it is being designed into systems in Europe, the USA and elsewhere in the World. This paper describes the latest advances in SpaceFibre technology for spaceflight applications including IP cores for chip designs and units for space application.

1 INTRODUCTION

SpaceFibre is the next generation of SpaceWire network technology for spacecraft on-board data-handling [1][2][3][4]. It runs over electrical or fibre-optic cables, operates at very high data rates, and provides in-built quality of service (QoS) and fault detection, isolation and recovery (FDIR) capabilities. Its high data rate per lane coupled with novel multi-lane technology enables SpaceFibre to achieve very high performance: in excess of 10 Gbit/s with current space qualified FPGAs and much higher in the near future. Its in-built error detection, isolation and recovery mechanisms enable rapid recovery from transient errors, without loss of data, providing high-availability. Its multi-lane hot and cold redundancy features support high reliability. These capabilities are built into the hardware of each SpaceFibre interface.

Data rates of tens of Gbit/s are required to support planned high data-rate payloads, including synthetic aperture radar and hyper-spectral optical instruments. In addition, mass-memory units require high performance networking to interconnect many memory modules.

This paper first looks at the SpaceFibre standard, describing each of its layers. It then mentions the use of SpaceFibre in another standard: SpaceVPX (VITA 78) where is acts advantageously as a backplane technology. To support SpaceFibre, STAR-Dundee has developed a comprehensive range of IP cores. These are described briefly in section 4 and their implementation footprints in various FPGA is considered in section 5.

2 SPACEFIBRE STANDARD

The SpaceFibre standard is now an approved ECSS standard – ECSS-E-ST-50-11C. This document specifies SpaceFibre by breaking it down into several distinct layers. The protocol stack for SpaceFibre is illustrated in Fig. 1. Each of the layers will now be described.

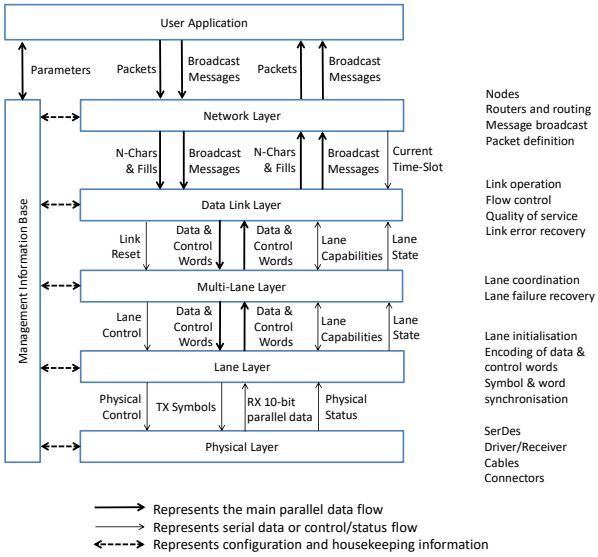

Fig. 1 SpaceFibre Protocol Stack

The Network layer protocol provides two services for transferring application information over a SpaceFibre network: the packet transfer service and the broadcast message service. The Packet Transfer Service transfers SpaceFibre packets over the SpaceFibre network, using the same packet format and routing concepts as SpaceWire. The broadcast message service broadcasts short messages carrying time and synchronisation information to all nodes on the network. The network layer is responsible for the specification of nodes, routing switches, routing mechanisms, message broadcast and the definition of packets.

The Data Link layer provides quality of service, flow control and error handing for a SpaceFibre link. It supports multiple virtual channels each having their own interface to the application and their own bandwidth allocation, priority and schedule. The Data Link layer sends packet information in small frames to facilitate multiplexing of packets from several virtual channels over one physical link. The Data Link layer is responsible for the overall operation of the link, the quality of service and link error recovery.

The Multi-Lane layer operates several SpaceFibre lanes in parallel to form a single link with higher data throughput. In the event of a lane failing the Multi-Lane layer provides support for graceful degradation,

automatically spreading the traffic over the remaining working links. It does this rapidly without any external intervention. The Multi-Lane layer is responsible for lane coordination and lane failure recovery.

The Lane layer initialises each individual lane and re-initialises the lane when an error is detected. Data is encoded into symbols for transmission using 8B/10B encoding and these symbols are decoded in the receiver. 8B/10B codes are DC balanced, supporting AC coupling of SpaceFibre interfaces. The Lane layer is responsible for the individual lanes providing lane initialisation and encoding of data and control words.

The Physical layer serialises the 8B/10B symbols and sends them over the physical medium. Both electrical cables and fibre-optic cables are supported by SpaceFibre. The physical layer is responsible for the serialisation and de-serialisation (SerDes), electrical driver and receiver, connectors and cables. Flight connectors and cables for both electrical and fibre-optic media are being developed.

The Management layer supports the configuration, control and monitoring of all the layers in the SpaceFibre protocol stack with a management information base.

3 SPACEVPX VITA78

SpaceVPX (VITA 78) builds on the ruggedized VPX standard, addressing the need for redundancy in spaceflight systems and focussing on conduction cooled racks [5]. SpaceVPX replaced the VMEbus control-plane of VPX with SpaceWire and enhanced versatility with a user defined serial data-plane interconnect. SpaceVPX concentrates on meeting a wide range of applications by defining sets of “backplane profiles”.

In the latest revision of SpaceVPX, which is currently in draft form, SpaceFibre has been included as a data-plane and control-plane technology. The virtual channels of SpaceFibre enable a single physical backplane network to be used to carry different classes or planes of traffic: i.e. the data-plane, control-plane and, to some extent, the management-plane of SpaceVPX. Furthermore, rapid and automatic graceful degradation of backplane interconnect in the event of a lane failure is now possible.

It is expected that the revised SpaceVPX standard will be release in 2020.

4 SPACEFIBRE IP CORES

To support users of SpaceFibre, STAR-Dundee has developed a comprehensive set of IP cores which are already being used in their first space missions and ASIC designs. The following IP cores are now available from STAR-Dundee targeted for radiation tolerant FPGA and ASIC implementation:

- Single-lane interface
- Multi-lane interface
- Single-lane routing switch

A multi-lane IP core is currently under development.

All these IP cores are fully configurable using VHDL generics and have been extensively validated. They are compliant to ECSS standard.

4.1 Single-lane interface

The STAR-Dundee SpaceFibre Single-Lane IP core has the following features:

- Designed by the team who created the standard.
- Easy to use with a protocol agnostic interface. No prior knowledge of SpaceFibre standard is required. The SpaceWire packet size, format and content is arbitrary.
- Optimised for low latency operation.
- Highly configurable, giving flexibility through generics in the VHDL source.
- Support lane rates up to 3.125 Gbit/s in RTG4 or Virtex-5QV and 6.25 Gbit/s in Kintex UltraScale
- Simple data interfaces based on standard input and output FIFO interfaces (32-bit AXI4-Stream).
- Independent user-defined data read and write AXI clocks.
- Automatically recovers from transient errors in less than 3 µs, without affecting the user data rate.
- Possibility to start one end of the link in a low-power mode waiting for the other end to become active.
- Data and broadcast babbling node protection.
- Data integrity and reliable data delivery for BER better than 10-5 and automatic lane disconnection when BER is worse than 10-5.
- Straightforward management interface, with optional statistics and debug signals.
- Validated in major FPGA families including radiation hard devices, e.g. Microsemi RTG4 and RTAX, and Xilinx Virtex-5QV, Spartan-6, Kintex-7 and Ultrascale KU060.

4.2 Multi-lane interface

The STAR-Dundee SpaceFibre Multi-Lane IP core has been designed to be easy to use, with a few configuration signals. In addition to the features of the Single-Lane IP Core, the Multi-Lane IP also features:

- Configurable number of independent lanes with cold and hot redundancy. Any number of lanes supported (up to 16).
- Automatic graceful degradation when link BW is reduced, with higher priority Virtual Channels being less affected.

- Hot redundant lanes recover from lane failures in less than 3 µs without user intervention.
- Lanes can be configured as unidirectional to save power and mass in asymmetric data flows.
- Wide AXI4-Stream interface to support slow user clock.
- Support lane rates up to 3.125 Gbit/s in RTG4 or Virtex-5QV and higher data rates in KU060 and PolarFire FPGAs

4.3 Single-lane routing switch

The SpaceFibre routing switch connects several nodes with SpaceFibre interfaces allowing them to talk to one another. Figure 4-1 shows the high-level architecture a SpaceFibre routing switch with a configurable number of SpaceFibre and SpaceWire ports, plus the configuration port [5]. Px stands for port X. Each SpaceFibre port has an individually configurable number of VCs whereas the SpaceWire ports only have a single VC. The configuration port uses the RMAP protocol to configure the routing table, the links and their corresponding QoS.

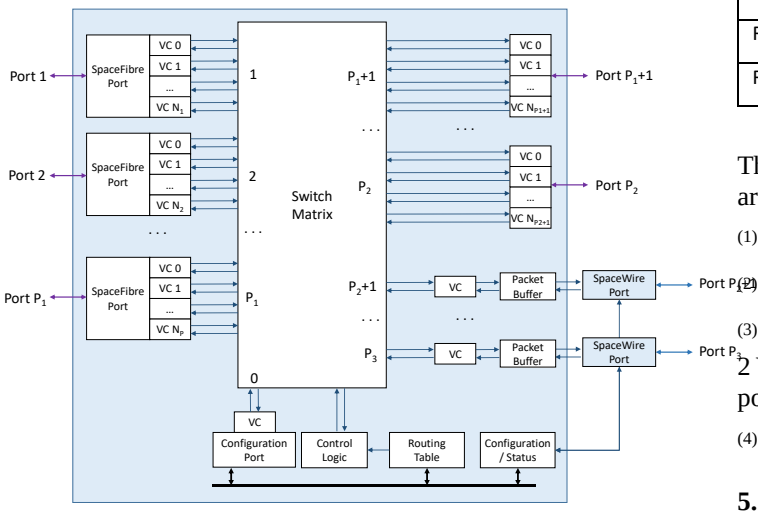

Figure 4-1 – SpaceFibre Router Block Diagram

The Router architecture is built around a non-blocking routing switch matrix with a number of ports. Each port can implement a number of VCs, each one comprising an input and an output VC buffer (VCB).

The STAR-Dundee SpaceFibre router switch IP core is available as a single-lane IP core and as a multi-lane IP core with a configurable number of lanes per port.

5 IMPLEMENTATION FOOTPRINT

The implementation footprint of the SpaceFibre IP core is one of its main features. The performance and capabilities of SpaceFibre are excellent, but this is of no use if the implementation footprint requires a large part of a radiation tolerant FPGA. In this section, the footprints of the STAR-Dundee SpaceFibre IP cores are provided for various configurations on different types of FPGA. The different manufactures of radiation tolerant FPGAs are studied in turn. Only FPGAs that incorporate SerDes are considered.

5.1 Microchip

The Microchip RTG4 is a radiation tolerant FPGA with 24 SerDes, which is being designed into many spaceflight units. A SpaceFibre interface takes a small corner of an RTG4 as detailed in Table 5-1. The figures for the multi-lane interface and routing switch will be added in the final version of this paper.

The RT-PolarFire is a new radiation tolerant FPGA from Microchip which is much larger than the RTG4 and includes higher speed SerDes. The resource utilisation of the PolarFire will be added in the final version of this paper.

Table 5-1: Resource utilisation of Microchip FPGAs

IP Core	Single-Lane Interface (1)	Multi-Lane Interface (2)	Single-Lane Router (3)
RTG4	2.9% / 2.1%(4)	TBA	TBA
RT-PolarFire	TBA	TBA	TBA

The specific IP core configurations detailed in the table are as follows:

(1) 2 Virtual Channels

(2) 4 Lanes and 2 Virtual Channels

(3) SpaceFibre Router with 8 SpaceFibre ports (each with 2 Virtual Channels) and embedded RMAP configuration port

(4) %LUT / % FF utilisation

5.2 Xilinx

The Virtex-5QV and the Ultrascale KU060 are Xilinx FPGAs which have been or are in the process of being qualified for space applications. In addition, various other Xilinx FPGAs have been or are being designed into spaceflight missions. The Virtex-5 and the Spartan-6 FPGAs have SerDes that are capable of 3.125 Gbit/s, while the Kintex-7 and Ultrascale FPGAs have SerDes that can operate at above 6.25 Gbit/s.

Table 5-2 shows the FPGA resources required for various IP cores on Xilinx FPGAs in terms of the percentage of the available LUTs and flip-flops (FF) on each FPGA. TMR is not included in these figures.

Table 5-2: Utilisation of Xilinx FPGAs

IP Core	Single-Lane Interface [1]	Multi-Lane Interface [2]	Single-Lane Router [3]
Virtex-5QV XQR5VFX130	3.1% / 3.3%[4]	9.6% / 11.7%	40.5% / 40.3%
Spartan-6 XC6SLX150T	3.4% / 1.4%	8.8% / 5.1%	38.4% / 16.8%
Kintex-7 XC7K325T	1.1% / 0.7%	3.3% / 2.2%	14.5% / 8.0%
Ultrascale KU060	0.6% / 0.4%	2.0% / 1.4%	8.6% / 4.9%

5.3 NanoXplore

Results for the NanoXplore NG-Large FPGA will be provided in the full paper. In the meantime, Figure 5-1 shows SpaceFibre running on the NG-Large FPGA.

Figure 5-1 SpaceFibre Running on NG-Large

Table 5-3: Utilisation of NanoXplore FPGAs

IP Core	Single-Lane Interface [1]	Multi-Lane Interface [2]	Single-Lane Router [3]
NG-Large	TBA[4]	TBA	TBA

6 CONCLUSIONS

SpaceFibre provides a high performance, high reliability, high availability network technology specifically designed for spaceflight applications. STAR-Dundee's SpaceFibre IP cores make it simple to provide network interfaces to instruments, data storage units, data compressors, other forms of data processor, downlink transmitters and to the control computer. The STAR-Dundee SpaceFibre router IP core provides the essential routing switch element interconnecting the other devices.

Instruments, processors and data-handling equipment are now being developed by many organisations with SpaceFibre interfaces.

7 REFERENCES

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