A Wideband Spectrometer in the Microsemi RTG4 FPGA

Steve Parkes[(1)],

[(1)]*University of Dundee, Space Technology Centre, Dundee, DD1 4HN, Scotland, UK.*

Email: s.m.parkes@dundee.ac.uk;

Martin Dunstan[(2)], Pete Scott[(2)], David Dillon[(2)], Alan Spark[(2)],

[(2)]*STAR-Dundee Ltd, STAR House, 166 Nethergate, Dundee, DD1 4EE, Scotland, UK.*

Email: martin.dunstan@star-dundee.com; pete.scott@star-dundee.com; david.dillon@star-dundee.com; alan.spark@star-dundee.com

Brian Ellison[(3)], Olivier Auriacombe[(3)]

[(3)]*STFC RAL Space, Harwell, Oxford, Didcot, OX11 0QX, UK*

Email: brian.ellison@stfc.ac.uk; olivier.auriacombe@stfc.ac.uk

ABSTRACT

A high-performance FFT processor for spectrometer applications in space has been designed, implemented and tested. The wideband spectrometer five (WBS V) implements a 1 k-point FFT in a Microsemi RTG4. Operating with dual 2.4 Gsamples/s ADCs it provides 2 GHz bandwidth with a FFT bin size of 2.4 MHz. The architecture, implementation and results of this spectrometer are described.

1 INTRODUCTION

A team of scientists and engineers from several organisations in the UK is working on an atmospheric limb sounding instrument to operate in the, largely unexplored, THz region of the electromagnetic spectrum which would be used to probe the physics and chemistry of the Mesosphere and Lower Thermosphere (MLT) region of the atmosphere. An engineering model of the THz radiometer [1] for the LOCUS (Linking Observations of Climate, the Upper-atmosphere, and Space-weather) instrument is being developed by Rutherford Appleton Laboratories (RAL), University College London (UCL), University of Leeds, STAR-Dundee and other partners in the UK. STAR-Dundee is responsible for the design of the backend spectrometer for this instrument.

STAR-Dundee has designed a high-performance Fast Fourier Transform (FFT) processor for spectrometer applications. The design has evolved through a series of wideband spectrometer (WBS) versions, which are listed below and illustrated in Figure 1.

- Initially, WBS I, using a single ADC (3 Gsamples/s) and DAC for testing;
- WBS II with two 3 Gsamples/s ADCs operating as an I and Q pair to give 2.8 GHz bandwidth which was processed with a 2k point FFT into around 1.5 MHz bands;
- WBS III an airborne version of the WBS II, built into a hermetically sealed box
- WBS IV a prototype spaceflight version using the Microsemi Igloo2 FPGA in preparation for a design with the radiation tolerant Microsemi RTG4 FPGA.
- WBS V, which uses the radiation tolerant Microsemi RTG4 FPGA, with commercial versions of radiation tolerant ADCs and other critical components, and operates at 2.4 Gsamples/s).

This paper describes the most recent development the WBS V which implements a 1 k-point FFT in a Microsemi RTG4 [2]. Operating with dual 2.4 Gsamples/s ADCs it provides 2 GHz bandwidth with a FFT bin size of 2.4 MHz. The architecture, implementation and results of this spectrometer are described.

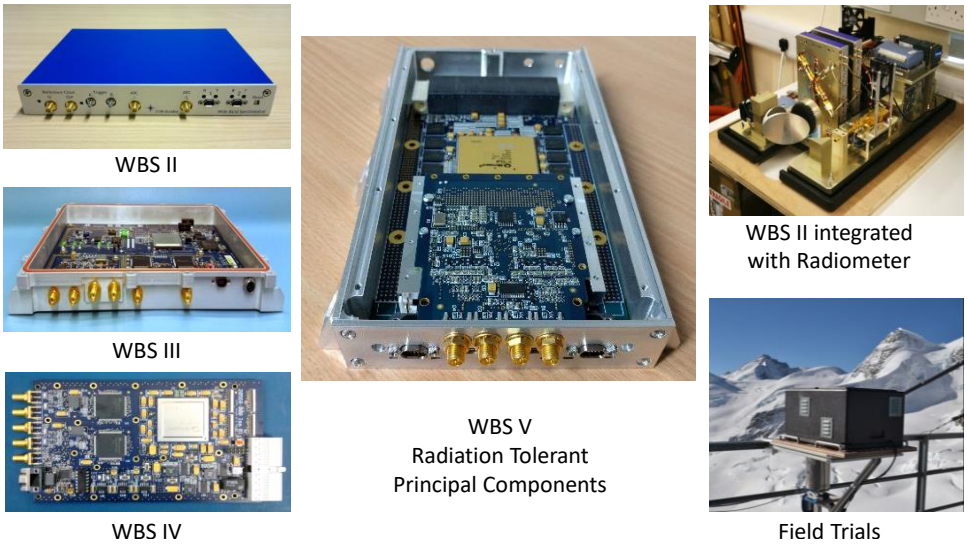


Figure 1: STAR-Dundee Spectrometers

2 WBS ARCHITECTURE

The overall architecture of a spectrometer capable of analysing 8 GHz bandwidth is illustrated in Figure 2. It is a hybrid spectrometer which comprises four individual wideband spectrometers (WBS V) which can each process 2 GHz bandwidth.

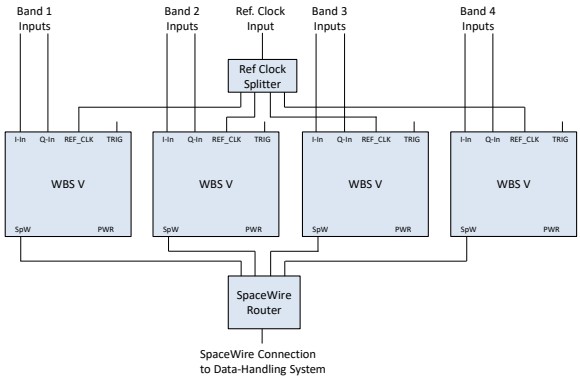


Figure 2: Spectrometer Architecture

Each WBS V unit is a complete 2 GHz bandwidth spectrometer with I and Q analogue inputs, a 10 MHz (nominal) reference clock and a SpaceWire interface [3][4] for configuration, control and monitoring and for retrieving the acquired power spectra. Several units can be interfaced to a SpaceWire router for connection via a single SpaceWire link to the spacecraft data-handling system. If the data rate is too high for a single SpaceWire link, multiple links can be used, or a SpaceWire to SpaceFibre bridge can be used which is able to carry data from twelve 200 Mbps SpaceWire links over a single SpaceFibre link [5].

The architecture of an individual WBS V unit is illustrated in Figure 3.

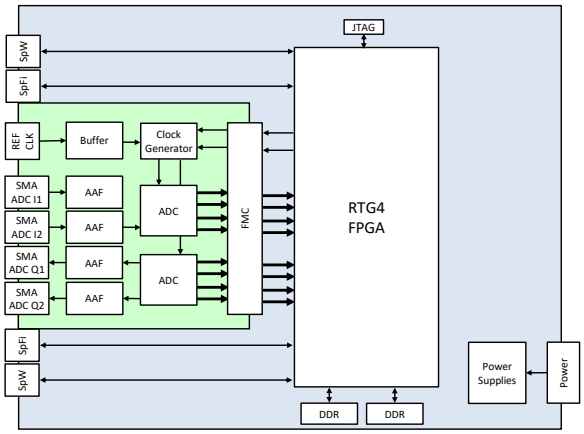


Figure 3: WBS V Unit Architecture

The WBS V unit comprises two boards: the SpaceVPX-RTG4 board (shown in blue) and the FMC-3GHz-ADC board which is a dual ADC board (shown in green). The main component on the SpaceVPX-RTG4 board is the radiation tolerant Microsemi RTG4 FPGA. This FPGA contains the ADC interface, FFT, power spectrum, accumulation, control and monitoring and SpaceWire interface circuitry. The FMC board contains two high speed ADCs which are operated as an I and Q pair at 2.4 Gsamples/s.

The analogue I and Q signals from the RF front-end are connected to two SMA connectors on the FMC board. Each input to the ADCs is a single-ended (unbalanced) input through an edge mount SMA connector and a weak anti-aliasing filter. The anti-aliasing filter is for test purposes only, since an external anti-aliasing filter is expected for a flight unit.

The clock signals for the ADCs and FPGA are generated on board using a clock distributor and clock manager (CDCM) chip and a 1.2 GHz VCXO. The

CDCM is locked to a 10 MHz reference clock from the FPGA. An external reference clock signal can also be used.

To operate the ADCs as an I and Q pair, it is necessary to ensure that the data outputs of the two ADCs are synchronised. This is done by resetting the data clocks of the two ADCs. This requires a Data CLK Reset signal which is synchronised to the 1.2 GHz clock requiring high speed logic.

Each ADC provides four de-interleaved data streams which are passed to the FPGA via the FMC connector. With a sample rate of 2.4 Gsamples/s the four data streams each operate at a data rate of 600 Msamples/s. These signals are transferred as low voltage differential signals (LVDS) to the FPGA. In total there are 128 data connections between the two ADCs and the FPGA. The four data streams are further de-interleaved within the FPGA.

A SpaceWire interface with support for the remote memory access protocol (RMAP) is provided for configuring, controlling and reading data from the WBS V. A trigger input or output interface is provided which may be used to trigger the operation of the WBS. A JTAG connector is provided on the SpaceVPX-RTG4 board for programming the Microsemi FPGA.

The power input for the WBS V board is nominally 5 volts which is provided via the backplane connector. However, this has been increased to 5.5 V to resolve an issue with voltage drop on the PCB. The voltages required in WBS V (3.3 V, 2.5 V, 1.9 V, 1.8 V and 1.2 V) are derived from the 5.5 V input by DC-DC convertors and regulators on the SpaceVPX-RTG4 and FMC boards.

2.1 WBS V Implementation

In this section the implementation of the WBS V is presented.

2.1.1 SpaceVPX-RTG4 board

The SpaceVPX-RTG4 board is a 3U SpaceVPX-Lite board. A photograph of the SpaceVPX-RTG4 board is shown in Figure 4. The main component on the board is the Microsemi RTG4 FPGA. Attached to two sides of the RTG4 FPGA (top and bottom in the photo) are two banks of DDR3 memory. These memory devices are EDAC protected with a 4-bit code for each 32-bit word. To the right of the RTG4 is the SpaceVPX-Lite connector, which can be used to plug the board in a SpaceVPX-Lite rack. Between this connector and the RTG4 is an array of capacitors and resistors which are used to configure the connections to the backplane connector, connecting many SpaceWire and/or SpaceFibre links to the backplane. Immediately to the left of the RTG4 is the FMC connector (in this photo the FMC connector has not been fitted, but the array of pads for the connector are clearly visible). The front panel on the far left of the board has two SpaceWire connectors (top and bottom) and two SpaceFibre connectors (middle). Between the FMC connector and the front panel are the various power supplies needed for the FPGA.

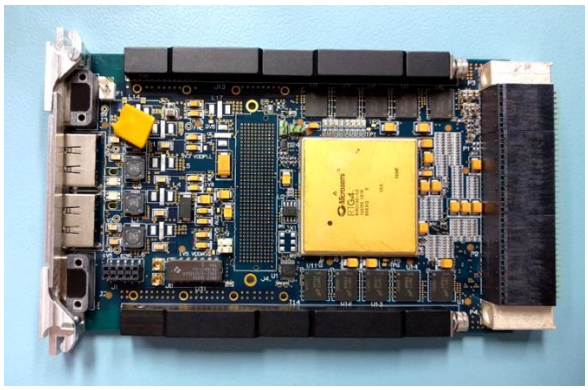


Figure 4: Photograph of the WBS V SpaceVPX-RTG4

The DDR memory is not used in the WBS V design. The backplane connector is only used to attach power to the board. The SpaceFibre connectors on the front panel are not used. A dual ADC board is attached to the FMC connector. The ADC data capture logic, the FFT, power detection, averaging, control and monitoring circuitry, and the SpaceWire interfaces with RMAP are all integrated in the FPGA.

The high sample-rate ADCs are implemented on an FMC daughterboard, which is shown in Figure 5.

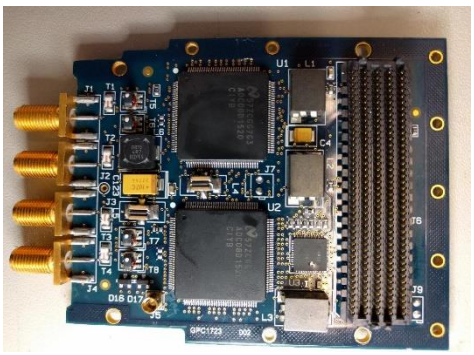


Figure 5: Photograph of the WBS V FMC-3GHz-ADC

The ADCs are the two large components in the middle of the board. The ADCs are operated at 2.4 Gsamples/s in the WBS V. On the left hand edge of the board are four SMA connectors which bring the analogue signals into the ADCs. Only two of these connectors are used in the WBS one for each ADC (I and Q). Each ADC provides 8-bit samples which are de-multiplexed to give four 8-bit outputs each running at a data rate of 600 Msamples/s. This slows the data rate to a speed which the FPGA can handle. The two sets of 32-bit data (one from each ADC) are provided as LVDS

signals (differential) and wired from the ADCs through the FMC connector to the FPGA. The FMC connector is on the far right of the board. A VCXO and clock distributor and clock manager (CDCM) chip are used to provide the 1.2 GHz double data-rate sampling clock for the ADCs. The VCXO is on the other side of the board. The CDCM is immediately to the left of the FMC connector and the second component up from the bottom. Next to the bottom left corner of the lower of the two ADCS can be seen a small MMCX connector (J5). This provides an external reference clock input to the board. The other components on the board are local point of load power supplies.

Figure 6 shows the FMC-3GHz-ADC board plugged into the SpaceVPX-RTG4 board and the assembly then mounted in the housing.

Figure 6: Photograph of the Integrated WBS V Unit

2.2 WBS V results

In this section the results of the WBS V are presented.

2.2.1 Development test set-up

A specially designed rack was used to house the WBS V during development and test, so that the two sides of the board were accessible to probe and monitor component operation. The operation of the WBS V spectrometer was tested using a signal generator connected to the inputs of the WBS V unit. The WBS V was controlled from a host computer via a SpaceWire link. The WBS V can be configured, controlled and monitored via SpaceWire and the results of data acquisition and processing can be retrieved and displayed.

2.2.2 Spectrometer results with signal generator input

Initially a complex 256-point FFT based spectrometer was implemented in the FPGA. The results of this spectrometer are illustrated in Figure 7 showing a 1000 frame integration of a 541MHz I/Q signal using rectangular and Hann window functions. The largest peak is the input signal fundamental frequency and the three other large peaks are harmonics of the input signal fundamental. The noise floor is around 45 dB below the main signal.

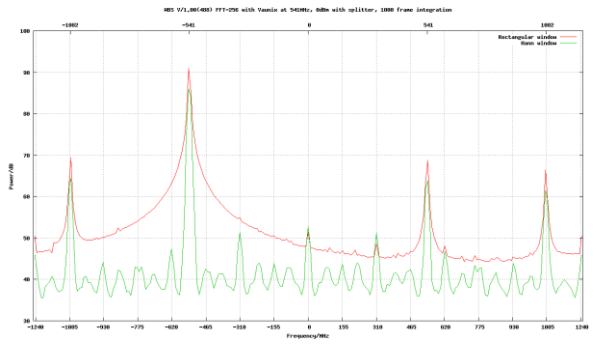


Figure 7: "First Light" power spectrum using 256-Point FFT of 541MHz tone

Following the success of the 256-point FFT, the 1024-point FFT was implemented. Tests were made with a signal generator at difference frequencies, windowing functions and integration times. The results of this design with two different window functions and 1

million frames of integration (0.4 seconds) are shown in Figure 8. The largest peak is the input signal fundamental frequency and the three other large peaks are harmonics of the input signal fundamental. The noise floor is around 56 dB below the main signal.

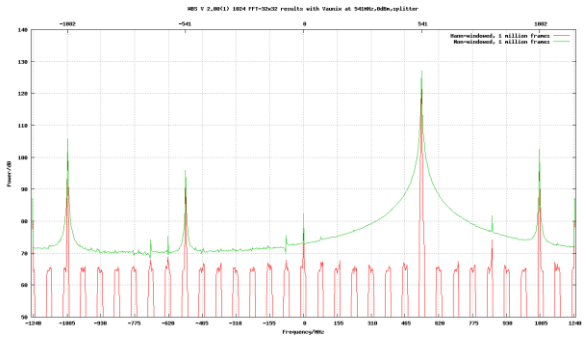


Figure 8: Power spectrum using 1024-point FFT with 1 million frame integration

2.2.3 Spectrometer results with a 360GHz receiver and molecular spectra

The WBS V unit sealed in its case was tested at RAL with a 360GHz receiver using nitrous oxide and methanol at different pressures to provide real-world testing and to compare against the WBS II unit. A labelled image of the test configuration and block diagram are shown in Figure 9.

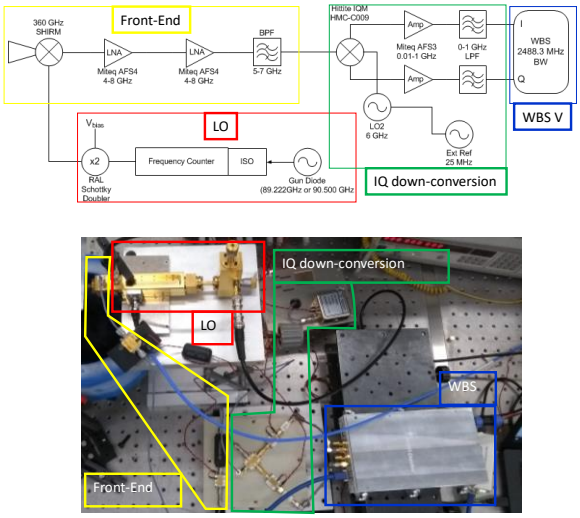
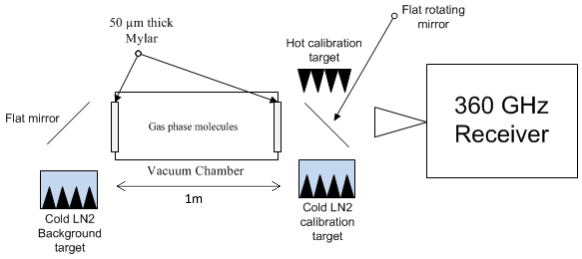


Figure 9: WBS V with 360GHz receiver

The gun diode was adjusted to select the local oscillator frequency around 90GHz. The precise setting depended on the molecular sample whose spectra was being captured. Note that both upper and lower side bands of the nominally 360GHz signal are captured by the WBS V. The targets were selected so that there were no lines in the upper side band or were much weaker than those in the lower side band (LSB).

The vacuum chamber into which the molecular samples were introduced is shown in Figure 10 showing how it is observed by the 360GHz front-end and the location of the cold target (blue bucket). During the tests the marked movable flat mirror was rotated down to block the vacuum target from the front-end and to reflect the cold target instead. A corrugated black plastic insert was placed in front of the mirror to act as a hot (room-temperature) target.



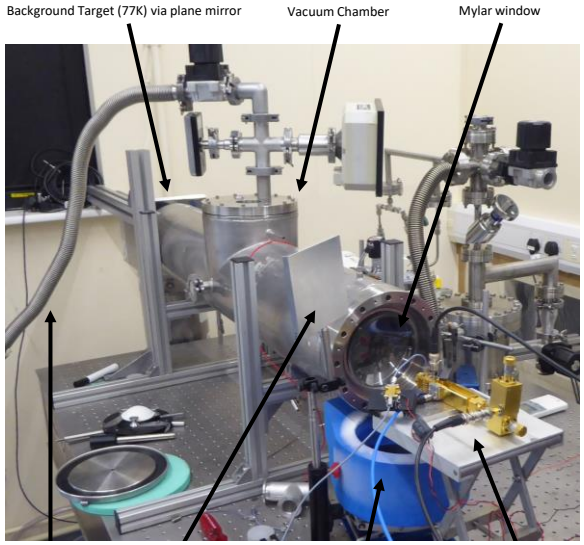


Figure 10: Vacuum chamber with cold targets, flat mirror and front-end

To capture spectra the chosen molecular sample was introduced to the vacuum chamber and the pressure adjusted to the required upper target. The WBS V was used to capture three spectra, typically using 2 second integration periods with the Hann windowing function. The first spectra was of the cold (liquid nitrogen) target in the blue bucket, the second of the hot target, and the third of scene (the vacuum chamber). The ratio of the difference in the power of the hot and cold targets (in each FFT bin) relative to the difference in their temperatures (nominally 291K and 77K respectively) allows the power in each bin of the spectrum of the vacuum target to be converted into a brightness temperature; the power of the cold target in each bin provides the temperature reference. Between each capture the flat mirror had to be moved and positioned

by hand so there are likely to be differences in the hot/cold results each time the spectra were captured.

A plot of a nitrous oxide sample showing the effects of pressure on the line width are shown in Figure 11. The spectra were captured using the WBS V.

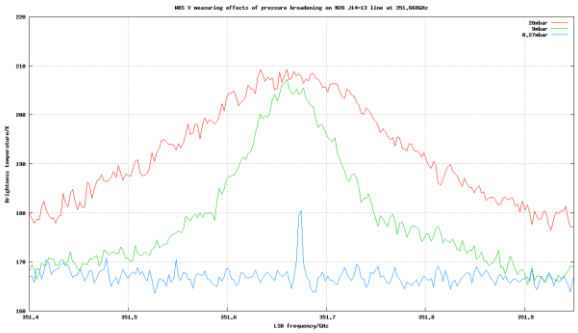


Figure 11: WBS V spectra of nitrous oxide line at different pressures

A plot comparing spectra captured with the WBS II and the WBS V is shown in Figure 12.

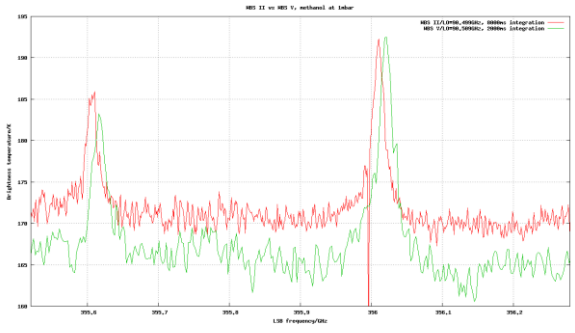


Figure 12: Methanol spectrum captured using WBS II and WBS V

The target spectral lines are at 355.603GHz and 356.007GHz. The downward spur in the WBS II plot at 355.996GHz is where the DC bin lies. The two spectra are shifted by about 10MHz relative to each other: this is due to small differences (around 2.5MHz) in the selection of the local oscillator frequency that occurred when the experiment was powered off to change the WBS units over.

These results show that the WBS V is successfully capturing 1024-point FFT power spectra with at least 56dB signal to noise ratio for pure sine wave tones and that it is able to capture real-world spectra using a high frequency receiver and I/Q down conversion.

3 CONCLUSIONS

A high-performance FFT based spectrometer has been designed, implemented and tested using radiation tolerant parts or commercial equivalents of radiation tolerant parts. A 1024-point FFT has been implemented in the Microsemi RTG4 FPGA. The processing power used is in the region of 100 GOPS enabling the 1024-point FFT to operate with I and Q inputs at a sample rate of 2.4 Gsamples/s. Achieving this high level of processing performance was not easy, but it clearly illustrates the power of the RTG4 for signal processing applications. Timing closure was achieved with SET filtering on and over the full temperature range.

The WBS V is a prototype device with a clear path to flight.

4 ACKNOWLEDGMENTS

The research leading to these results has received funding from the CEOI-ST, UK Space Agency and ESA.

5 REFERENCES

[1] S.P. Rea, et al, “The Low-Cost Upper-Atmosphere Sounder (LOCUS)”, 26th International Symposium on Space Terahertz Technology, Cambridge, MA, 16-18 March 2015.

[2] Microsemi, “RTG4 FPGAs - High-Speed RT FPGAs for Signal Processing Applications”, http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtg4 (last visited 11th Feb 2018).

[3] ECSS Standard ECSS-E-ST-50-12C, “SpaceWire, Links, Nodes, Routers and Networks”, Issue 1, European Cooperation for Space Data Standardization, July 2008, available from http://www.ecss.nl.

[4] S. Parkes, “SpaceWire User’s Guide”, ISBN: 978-0-9573408-0-0, STAR-Dundee, 2012, available from https://www.star-dundee.com/knowledge-base/spacewire-users-guide (last visited 11th Feb 2018).

[5] S. Parkes, A. Ferrer Florit and A. Gonzalez Villafranca, “SpaceFibre Standard”, Draft K2, University of Dundee, December 2017.