Design and Test of SpaceFibre Interfaces in FPGAs

Steve Parkes[(1)], Chris McClements[(1)], David Gibson[(1)], Stephen Mudie[(1)],

Albert Ferrer Florit[(2)], Alberto Gonzalez Villafranca[(2)], Marti Farras Casas[(2)]

[(1)] STAR-Dundee Ltd.

[(2)] STAR-Barcelona S.L.

Tel: +44 1382 225613

steve.parkes@star-dundee.com

Abstract - SpaceFibre is a very high performance, high reliability and high availability network for spaceflight applications. The latest advances in SpaceFibre technology for spaceflight applications are described, including IP cores for use in radiation tolerant FPGAs and SpaceFibre test equipment that can be used to accelerate the development of next generation payload processing systems.

Keywords - SpaceFibre, SpaceWire, RTG4, PolarFire, KU060, SerDes, FPGA, Radiation Tolerant.

INTRODUCTION

SpaceFibre is the next generation of SpaceWire network technology for spacecraft on-board data-handling [1][2][3][4]. It runs over electrical or fibre-optic cables, operates at very high data rates, and provides in-built quality of service (QoS) and fault detection, isolation and recovery (FDIR) capabilities. Its high data rate per lane coupled with novel multi-lane technology enables SpaceFibre to achieve very high performance: in excess of 10 Gbit/s with current space qualified FPGAs and much higher in the near future. Its in-built error detection, isolation and recovery mechanisms enable rapid recovery from transient errors, without loss of data, providing high-availability. Its multi-lane hot and cold redundancy features support high reliability. These capabilities are built into the hardware of each SpaceFibre interface.

The SpaceFibre standard is now an approved ECSS standard – ECSS-E-ST-50-11C [1].

SpaceFibre IP Cores

To support users of SpaceFibre, STAR-Dundee has developed a comprehensive set of IP cores which are already being designed into their first spaceflight equipment and used in ASICs. The following IP cores are now available from STAR-Dundee targeted for radiation tolerant FPGA and ASIC implementation:

- Single-lane interface
- Multi-lane interface
- Single-lane routing switch

A multi-lane IP core is currently under development.

All these IP cores are fully configurable using VHDL generics and have been extensively validated. They are compliant to ECSS standard.

a. Single-lane interface

The STAR-Dundee SpaceFibre Single-Lane IP core has the following features:

- Easy to use with a protocol agnostic interface. No prior knowledge of the SpaceFibre standard is required. The SpaceWire packet size, format and content is arbitrary.
- Validated in major FPGA families including radiation hard devices, e.g. Microsemi RTAX, RTG4 and PolarFire, and Xilinx Virtex-5QV, Spartan-6, Kintex-7 and Ultrascale KU060.
- Supports lane rates up to 3.125 Gbit/s in RTG4 and Virtex-5QV, and 6.25 Gbit/s in Kintex UltraScale and RT-PolarFire.
- Highly configurable, giving flexibility through generics in the VHDL source.
- Simple data interfaces based on standard input and output FIFO interfaces (32-bit AXI4-Stream).
- Independent user-defined data read and write AXI clocks.
- Straightforward management interface, with optional statistics and debug signals.
- Automatically recovers from transient errors in less than 3 µs, without affecting the user data rate.

- Possibility to start one end of the link in a low-power mode waiting for the other end to become active.
- Optimised for low latency operation.
- Data and broadcast babbling node protection.
- Data integrity and reliable data delivery for BER better than 10-5, and automatic lane disconnection when BER is worse than 10-5.

b. Multi-lane interface

The STAR-Dundee SpaceFibre Multi-Lane IP core has been designed to be easy to use, with a few configuration signals. In addition to the features of the Single-Lane IP Core, the Multi-Lane IP also features:

- Configurable number of independent lanes with cold and hot redundancy. Any number of lanes supported (up to 16).
- Automatic graceful degradation when link BW is reduced, with higher priority Virtual Channels being less affected.
- Hot redundant lanes recover from lane failures in less than 3 µs without user intervention.
- Lanes can be configured as unidirectional to save power and mass in asymmetric data flows.
- Wide AXI4-Stream interface to support slow user clock.

c. Single-lane routing switch

The SpaceFibre routing switch connects several nodes with SpaceFibre interfaces allowing them to talk to one another. The Router architecture is built around a non-blocking routing switch matrix with a number of SpaceFibre ports. Each port can implement a number of virtual channels (VCs), each one comprising an input and an output VC buffer. A configuration port uses the RMAP protocol to configure the routing table, the links and their corresponding QoS. The STAR-Dundee SpaceFibre router switch IP core is available as a single-lane IP core and will soon be available as a multi-lane IP core with a configurable number of lanes per port.

Implementation Footprint

The implementation footprint of the SpaceFibre IP core is one of its main features. The performance and capabilities of SpaceFibre are excellent, but this is of no use if the implementation footprint requires a large part of a radiation tolerant FPGA. In this section, the footprints of the STAR-Dundee SpaceFibre IP cores are provided for various configurations on different types of FPGA. The different manufacturers of radiation tolerant FPGAs are considered in turn. Only FPGAs that incorporate SerDes are considered.

The Virtex-5QV and the Ultrascale KU060 are Xilinx FPGAs which have been or are in the process of being qualified for space applications. In addition, various other Xilinx FPGAs have been or are being designed into spaceflight missions. The Virtex-5 and the Spartan-6 FPGAs have SerDes that are capable of 3.125 Gbit/s, while the Kintex-7 and Ultrascale FPGAs have SerDes that can operate at above 6.25 Gbit/s.

The Microchip RTG4 is a radiation tolerant FPGA with 24 SerDes, which is being designed into many spaceflight units. The RT-PolarFire is a new radiation tolerant FPGA from Microchip which is much larger than the RTG4 and includes higher speed SerDes.

The resource utilization for the Xilinx and Microchip FPGAs are provided in Table 1. Triple-mode redundancy is not included in these figures.

Table 1: Resource utilization in various FPGAs

IP Core	Xilinx Virtex-5QV XQR5VFX130	Xilinx Spartan-6 XC6SLX150T	Xilinx Kintex-7 XC7K325T	Xilinx Ultrascale KU060	Microchip RTG4	Microchip RT-PolarFire
Single-Lane Interface [1]	3.1% / 3.3%[4]	3.4% / 1.4%	1.1% / 0.7%	0.6% / 0.4%	2.9% / 2.1%	TBA
Multi-Lane Interface [2]	9.6% / 11.7%	8.8% / 5.1%	3.3% / 2.2%	2.0% / 1.4%	TBA	TBA
Single-Lane Router [3]	40.5% / 40.3%	38.4% / 16.8%	14.5% / 8.0%	8.6% / 4.9%	TBA	TBA

The specific IP core configurations detailed in the table are as follows:
[1] 2 Virtual Channels
[2] 4 Lanes and 2 Virtual Channels
[3] SpaceFibre Router with 8 SpaceFibre ports (each with 2 Virtual Channels) and embedded RMAP configuration port
[4] %LUT / % FF utilization
TBA to be provided in the final paper/presentation

SpaceFibre Test and Development Equipment

The STAR-Ultra PCIe is an 8-lane PCIe Gen 3 board with two quad-lane interfaces. It has two quad-lane SpaceFibre interfaces.

The STAR-Ultra PCIe has three main functions:

- Sending data from a host PC to an element under test over SpaceFibre at up to 10 Gbit/s
- Receiving data from an element under test to a host PC over SpaceFibre at up to 10 Gbit/s
- Capturing and analysing data travelling over SpaceFibre to support element and system-level debugging

The performance of the STAR-Ultra PCIe is as follows:

- Maximum data rate per lane 6.25 Gbit/s
- Maximum data rate per link over 10 Gbit/s
- Maximum data rate to host PC over 10 Gbit/s

The STAR-System software that comes with the STAR-Ultra PCIe includes:

- High-performance software drivers (>10 Gbit/s)
- SpaceFibre configuration and control software
- User-data transmit and receive applications
- Link analyser control and display software

The SpaceFibre link analyzer software provides clear visibility of the various protocol layers of SpaceFibre and enables rapid inspection of large volumes of data. There are several views of the data provided which are automatically synchronized with one another:

Word View shows the individual symbols and words that are used to initialize and send data over a SpaceFibre link and to recover communications after a failure. It is possible to scroll up and down and to search for specific symbols and words. This view is particularly helpful when debugging the low-level of SpaceFibre.

Frame View shows each virtual channel in a separate column and the frames that are flowing over the link. Frames are multiplexed over the link to provide the separate virtual channels and to support the quality of service of the virtual channels.

Packet View shows the packet data flowing over each of the virtual channels. The packet data can be shown in various formats.

Navigation View is used to navigate around the large amount of data that can be captured by the link analyzer, see Figure 1. Time progresses from left to right and each virtual channel is shown as a series of rows. Each trace shows the volume of user data that is flowing over the link over each of the virtual channels.

Figure 2 shows what happens as the user zooms into the data. The two vertical black lines are the click and drag zoom region that is being selected. Dynamically the display changes to showing the frames and packets, in dark blue, as well as the grey data volume line. It is now possible to see that each of the dips in the traffic volume corresponds to the virtual channel stopping sending frames. As the user scrolls to the left or right or picks a point to look at using the cursor, the display will centre on that point and the word, frame and packet views will all focus on that point. This provides a simple and intuitive, but powerful means of scanning through vast amounts of data looking for potential anomalies and then instantly being able to see the full detail.

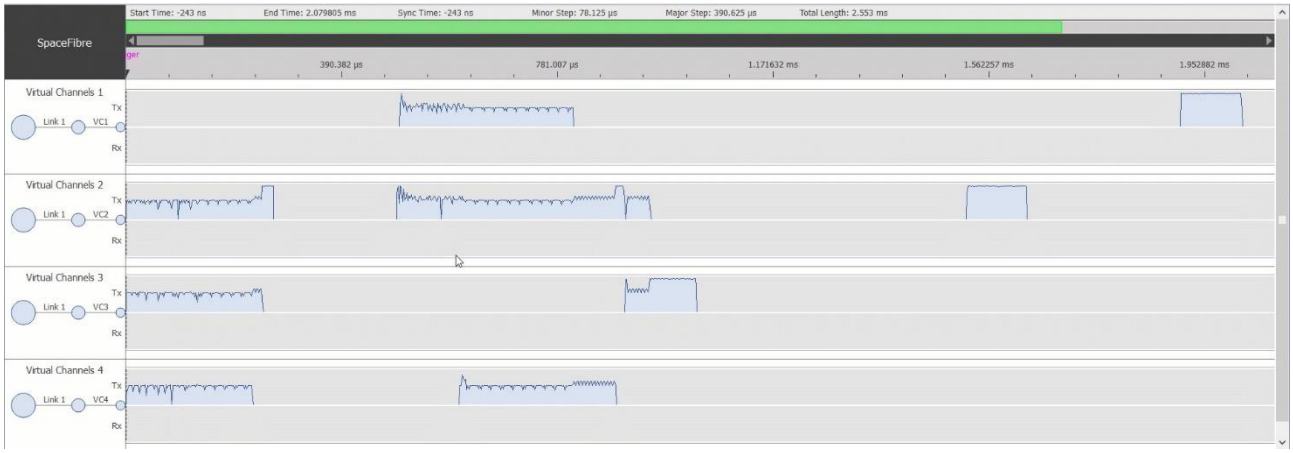

Figure 1: ***STAR-Ultra PCIe Link Analyser Network Summary View***

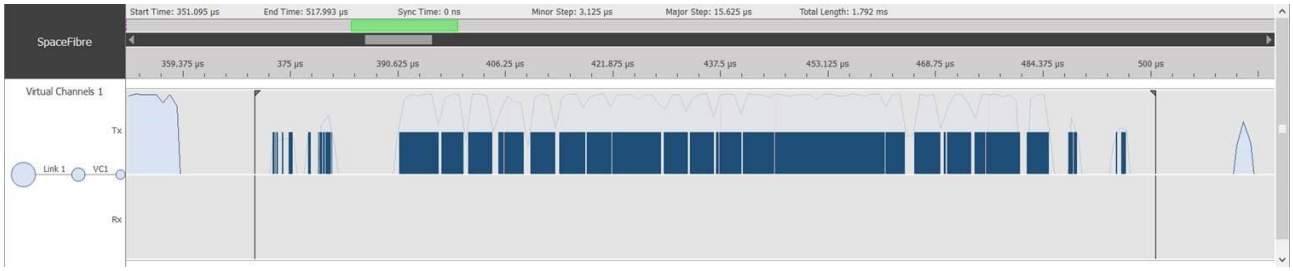

Figure 2: ***STAR-Ultra PCIe Link Analyser Network Summary View and Detailed View***

Conclusion or Summary

SpaceFibre is now being integrated in many spacecraft equipment designs. It provides high-performance, high-reliability and high-availability, and has a small footprint in an FPGA. This makes it ideal for high-speed interconnect for connecting instruments, mass-memory, downlink transmitter, data compressor, payload processors and other equipment together on-board a spacecraft. The necessary IP cores and test equipment are available and being used to support such developments.

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