TESTING SPACEWIRE SYSTEMS ACROSS THE FULL RANGE OF PROTOCOL LEVELS WITH THE SPACEWIRE PHYSICAL LAYER TESTER.

Session: SpaceWire test and Verification

Long Paper

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ABSTRACT

STAR-Dundee have previously reported on test equipment which is capable of testing the Network, Packet, Exchange, Character and parts of the Signal level of the SpaceWire standard. This paper introduces the SpaceWire Physical Layer Tester (SPLT), which is a new tool designed to test, validate and verify a SpaceWire system across all levels covered by the SpaceWire standard.

Two SpaceWire ports on the SPLT employ a special LVDS interface which allows the transmitted signals to be deliberately and measurably manipulated to test the capability of a unit under test (UUT) to receive signals of varying quality. The SPLT SpaceWire drivers offer full, independent control of voltage offset and amplitude for data and strobe pairs. Skew can be introduced both in-pair and between data-strobe pairs. Slew rates can be individually configured on each half of the differential pairs. To facilitate acquisition of an eye-diagram, the signal received on the termination resistors on these ports is buffered on external connectors to allow easy interfacing to an oscilloscope. This allows a comprehensive suite of tests to be performed through the UUT SpaceWire port without the need to open the unit.

In addition to the LVDS interface, the SPLT also implements many of the capabilities of existing STAR-Dundee devices: Link Analyser Mk2, Conformance Tester and USB Brick in addition to the packet generator and checker capabilities of the newly announced SpaceWire EGSE. A pair of Gigabit Ethernet ports and a USB 2.0 port in addition to an API allow for great flexibility in interfacing the SPLT to existing test environments. The device is rack mountable in a 1U, half width format.

1 EXISTING TECHNIQUES FOR TESTING THE PHYSICAL AND SIGNAL LAYER

1.1 INTRODUCTION

The SpaceWire Standard is defined across six levels ranging from the Physical level up to the Network level. A successful SpaceWire system must be implemented in a way which conforms to the specifications laid out across all of these levels. A range of existing techniques can be implemented to analyse the performance of such a system at the physical and signal layer. A more detailed overview of the devices and test techniques discussed in this section can be found in [1].

1.2 TIME DOMAIN REFLECTOMETRY

Time Domain Reflectometry is used to evaluate the performance of connectors, differential pair traces on Printed Circuit Boards (PCB), backplanes, cables and any other media which is used to transmit SpaceWire LVDS electrical signals. A pulse is transmitted down a SpaceWire differential pair and the analysis of the reflections can show up impedance discontinuities or incorrect termination of the line. An appropriate interface to the SpaceWire port is required to inject the test signals and measure the responses.

1.3 EYE PATTERN MEASUREMENT & SPECTRUM ANALYSIS

Measuring the eye-pattern of a SpaceWire signal using a high speed oscilloscope gives insight to the transmitter characteristics of the unit under test. The signal's rise and fall times and jitter can be observed. A mask can be applied to the opening of the eye for a sustained test period to verify that the signal remains in a valid region. Eye pattern measurement can also be employed to measure Data-Strobe skew characteristics by measuring the Data eye pattern when triggering on the Strobe signal and vice-versa. A Spectrum Analyser can be used to display the power spectrum of a SpaceWire signal being transmitted from a UUT and analyse parameters such as drift and jitter.

One of the biggest difficulties in performing Spectrum Analysis or Eye Pattern measurements on a SpaceWire system is that it requires probes to be fixed to the LVDS termination resistors in the receiver. It is often undesirable or not permitted to remove the case of flight equipment and attach probes onto the relevant components. A further difficulty is that these tests work best when pseudo-random bit streams (PRBS) are being analysed. It may be difficult to configure a unit under test to generate such a condition.

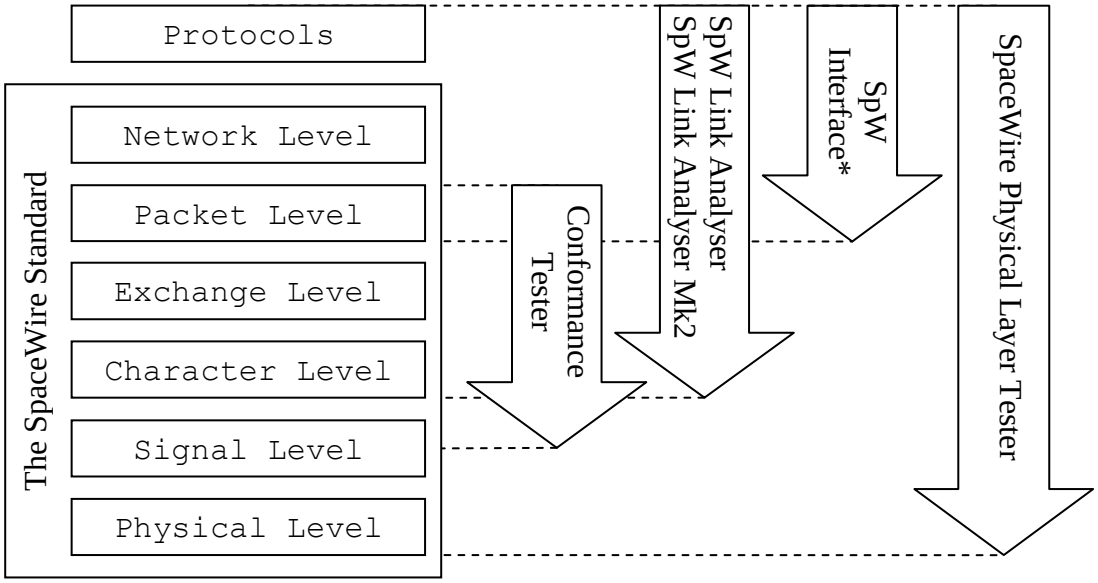
1.4 BIT ERROR RATE TESTING (BERT)

BERT systems will typically use a transmitter to generate a PRBS or pre-programmed bit sequence for transmission to the UUT. A receiver in the BERT system will compare the received signal to an expected signal and flag any bit-errors that are detected. One difficulty with these systems is that an interface from the transmitter/receiver to a SpaceWire port would have to be implemented. It also assumes that the unit under test can conveniently output PRBS test data through a loopback mode.

2 THE STAR-DUNDEE SPACEWIRE PHYSICAL LAYER TESTER

2.1 TESTING ACROSS THE SPACEWIRE STANDARD

STAR-Dundee currently supply a range of test equipment which tests across most, but not all levels of the standard. This is summarised in Figure 1.



*Includes EGSE, SpW Brick, SpW PCI Mk2, SpW cPCI Mk2, SpW PMC Mk2, SpW PCI Express and SpW Router Mk2.

Figure 1: Testing, Monitoring and Verifying SpaceWire systems across the SpaceWire standard with STAR-Dundee test equipment.

2.2 OVERVIEW OF THE SPACEWIRE PHYSICAL LAYER TESTER

The unique feature of the STAR-Dundee SPLT is the capability of manipulating the analogue characteristics of the output LVDS signals. This facilitates the analysis of what the UUT is capable of successfully receiving. The severity of skew, slew, swing, common-mode and jitter can be controlled to mimic a range of physical media, environments and device output characteristics. The operation and capabilities of these special LVDS drivers is explained in Section 4. The SPLT also features the capability to connect a high speed oscilloscope via SMA connectors on the front panel in order to observe the received SpaceWire signals. High speed analogue buffers are utilised to buffer the signal close to the termination resistors allowing the SPLT to receive and decode the SpaceWire signals whilst they may be simultaneously monitored by an oscilloscope.

The SPLT is a 1U rack mountable ½ width device which interfaces to a host PC through either USB 2.0 or one of its 2 Gigabit Ethernet ports. A Mictor connector allows a logic analyser to interface to the device's inbuilt STAR-Dundee Link Analyser Mk2 [2]. An enhanced version of the STAR-Dundee Conformance Tester [3] allows advanced conformance testing of the physical layer to be performed.

3 PERFORMING TESTS WITH THE SPACEWIRE PHYSICAL LAYER TESTER

3.1 INTRODUCTION

A range of tests can be performed with the SPLT operating in different modes.

3.2 IN-LINE MARGIN ANALYSIS

The SPLT is connected between two SpaceWire UUTs in the same way a STAR-Dundee Link Analyser would be connected. This configuration is shown in Figure 2.

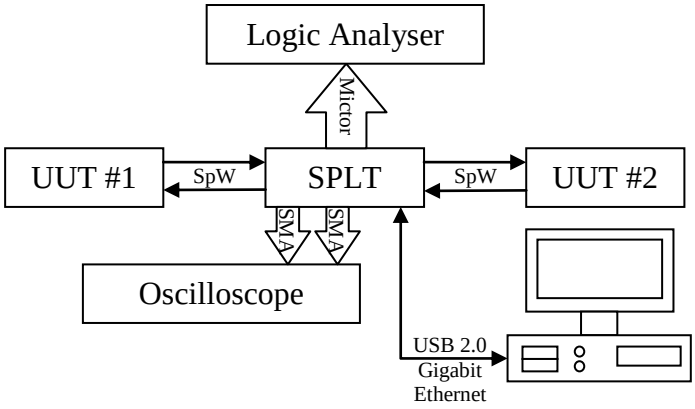


Figure 2: Using the SPLT to perform in-line margin analysis between two devices under test.

When operating in in-line analysis mode, the two UUTs will communicate as normal, sending and receiving data to each other. The SPLT buffers the incoming signals on one SpaceWire port and then drives them out through the analogue LVDS drivers on the other SpaceWire port. The SPLT can then manipulate the SpaceWire signals in one, or both, directions to explore the receive margins of either, or both, UUT devices.

3.3 LOOP-BACK MARGIN ANALYSIS

In loop-back configuration, the SPLT is connected to a single UUT as shown in Figure 3.

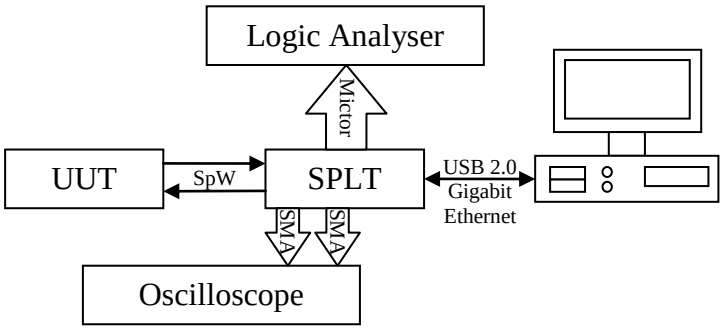


Figure 3: Using the SPLT to perform loop-back margin analysis, conformance testing, pattern generation & checking on a single UUT. This setup can also be implemented to use the SPLT as a SpaceWire interface to a Host PC.

In loop-back analysis, the SPLT receives data from the UUT and loops the data back through the same SpaceWire port. The LVDS transmitters can manipulate the data to test the receive margins of the UUT. The signals received from the UUT are buffered by the SPLT and made available for analysis on an oscilloscope. Loop back SpaceWire data is decoded onto the Mictor connector for easy interface to a Logic Analyser. Loop-back analysis requires the UUT to be able to start a SpaceWire link and to send and receive SpaceWire commands.

3.4 CONFORMANCE TESTING

The SPLT implements an advanced version of the STAR-Dundee Conformance Tester with additional tests which take advantage of the analogue LVDS driver capabilities of the SPLT. The test environment is set up in the same configuration as Figure 3.

3.5 PATTERN GENERATION AND CHECKING

A series of Packets can be pre-programmed into the SPLT for transmission as well as a series of expected packets that should be returned by the UUT. The SPLT can be set up to mimic a SpaceWire device that will be interfaced to the UUT. The test packets are transmitted from the SPLT at high speed and the UUT response checked against the pre-defined expected response. Any errors in the received bit-stream will then be flagged up by the SPLT.

3.6 SPACEWIRE INTERFACE WITH RMAP CAPABILITY

In SpaceWire interface mode, the SPLT is used to send and receive SpaceWire packets to a UUT from a PC through either USB 2.0 or Gigabit Ethernet connections. In this way, the SPLT works in a similar fashion to the STAR-Dundee SpaceWire Brick, but with added capabilities of LVDS margin testing. An RMAP target provides memory space which can be written to or read from by the UUT.

3.7 DETECTING ERRORS AND DEBUGGING CAPABILITIES OF THE SPLT

As the output LVDS signals are progressively degraded, bit errors on one, or both of the interfaced UUTs become increasingly likely. SpaceWire bit errors will manifest themselves as link disconnects due to detection of parity errors. Errors which are not detected by parity may still be picked up by implemented protocol features such as the RMAP cyclic redundancy check (CRC). The SPLT inbuilt Link Analyser Mk2 could then be triggered on detection of an RMAP header which reports a CRC failure.

The analogue signals received at the inputs of each SpaceWire port are buffered by the SPLT. An oscilloscope can be used to monitor the received data and strobe signals from both SpaceWire ports simultaneously. The SpaceWire data flowing through the SPLT SpaceWire ports is decoded by an inbuilt Link Analyser Mk2 and the characters are output on a Mictor connector suitable for interfacing to a Logic Analyser. A Host PC can be used to control the inbuilt SPLT Link Analyser Mk2 to trigger, store and read out captured data.

4 OPERATION OF THE LVDS DRIVERS

Figure 4 shows the components of the LVDS driver which are employed to manipulate the output of the SpaceWire signals.

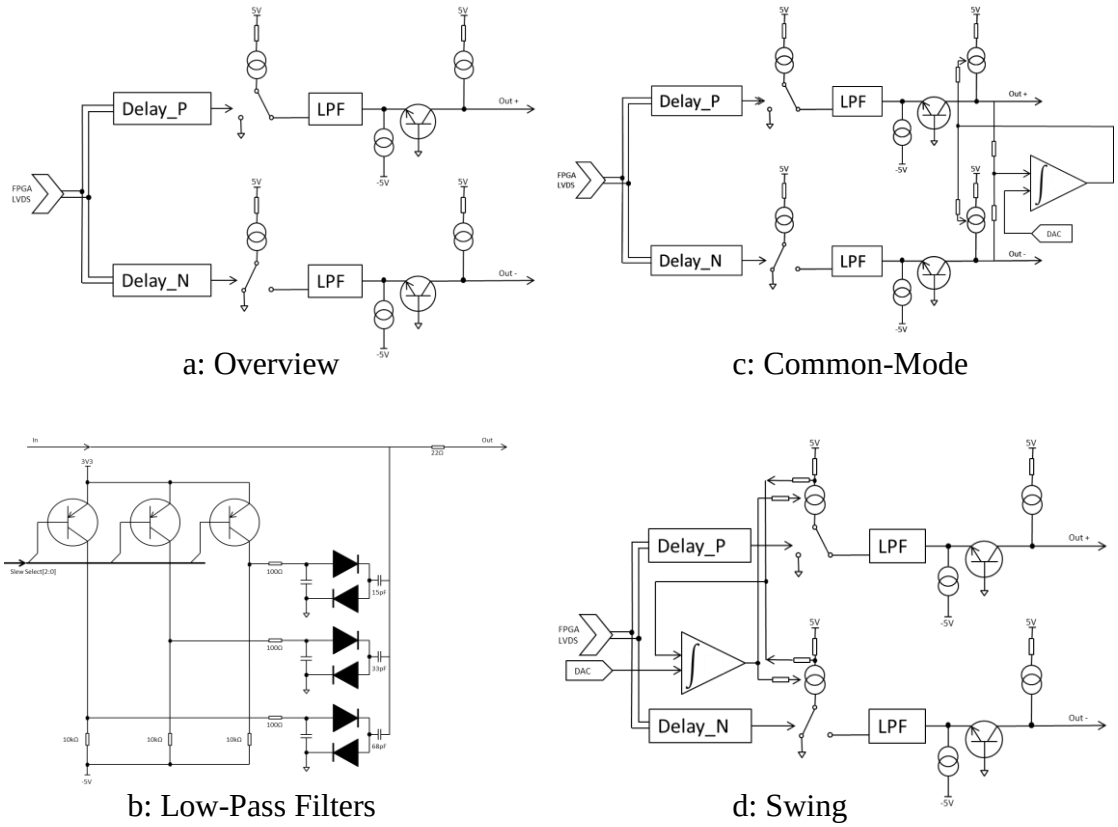


Figure 4: Operation of the LVDS driver circuitry. Figure 4a gives a simplified overview of the LVDS driver chain. b shows the operation of the low-pass filter (LPF) component. c and d respectively show the circuitry responsible for controlling the common-mode and swing of the LVDS signalling.

4.1 MANIPULATION OF SKEW AND JITTER USING THE DELAY LINES

Delay lines on the positive and negative transmission lines allow the measurable introduction of in-pair and Data-Strobe skew to a resolution of 10ps. A SpaceWire device should state what its maximum operating frequency is for a given Data-Strobe skew. The SPLT allows this test to be performed directly. Cables will typically state how much skew there is per unit length of cable. This information can be used to simulate different cables of different lengths.

Jitter can also be introduced into any of the delay lines. This can be used to simulate a device's stated jitter characteristics as well as deterioration of signal caused by electromagnetic interference (EMI).

4.2 MANIPULATION OF SLEW USING THE LOW PASS FILTERS

The low pass filters work by switching a combination of 3 capacitors of differing capacitance into or out of of the chain. This allows for eight different levels of slew to be introduced to a signal. Signal slew is typically caused by the capacitive effect of

the cable down which the signal travels. This allows the SPLT to simulate different cable characteristics such as length and mutual capacitance.

4.3 CONTROLLING THE SWING AND COMMON-MODE OF THE LVDS SIGNALLING

Digital to Analogue Converters (DACs) are used to set both the swing and the common-mode voltage by controlling reference voltage levels into operational amplifiers. Additional calibration voltages are used to ensure that both positive and negative components of the LVDS pair swing by the same magnitude about an equal common-mode.

Modification of the swing of the output signal simulates attenuation of the SpaceWire signal as it propagates through pcb traces and cables from transmitter to receiver. Attenuation can be simulated for media of differing lengths.

SpaceWire is not DC balanced and requires adequate common grounding between the communicating systems. Imbalances in ground plane, or power supply voltages between units could cause the DC level of the LVDS signalling to drift. The LVDS can test the permitted margins of this drift by manipulating the common-mode voltage of the output signal.

4.4 NO SINGLE POINT OF FAILURE

The design of the SPLT electronics guarantees that there will be no single point of failure on the SPLT that could damage SpaceWire equipment to which it is connected.

5 MEASURMENTS FROM THE LVDS DRIVERS

In order to demonstrate the capabilities of the SPLT, the Data and Strobe signals of a SpaceWire port were driven with a 25MHz square wave before manipulation by the analogue-electronics. The SpaceWire port was looped back into the analogue SpaceWire buffers on the SPLT so that an oscilloscope could be used to analyse the outputs. Screenshots from the oscilloscope measurements are presented in Figure 5 to show the discrete sources of signal disruption that the SPLT can introduce. Figure 5h then shows these sources combined to give a typical margin-testing waveform.

6 CONCLUSION

The SpaceWire Physical Layer Tester incorporates and builds upon established STAR-Dundee test products: the Link Analyser Mk2, the Conformance Tester and SpaceWire interface devices. Whether used with just a host PC, or in conjunction with a high speed oscilloscope and logic analyser, the SPLT can be connected in a variety of configurations to test SpaceWire systems. The ability to measurably deteriorate the SPLT output LVDS signals and to easily measure the input signals on an interfaced oscilloscope allows the SPLT to test, validate and verify SpaceWire systems from the physical and signal layer of the SpaceWire standard, right up to any protocols which are running on top of the SpaceWire standard.

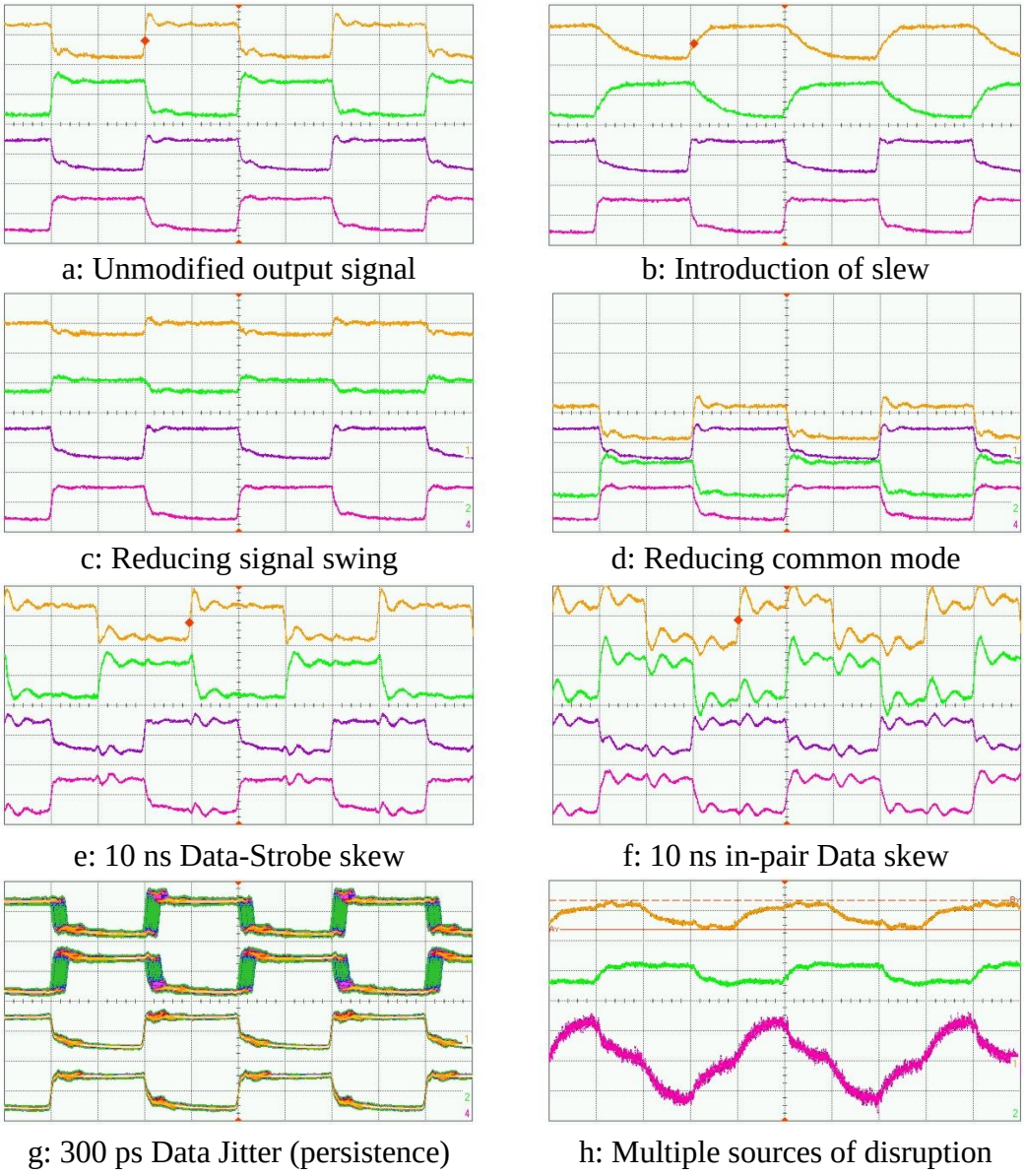


Figure 5: Measuring the different methods of deteriorating the LVDS signals from the SPLT. In these measurements, the Data (top pair) is manipulated with the strobe (bottom pair) untouched. Figure 5h omits the Strobe signal and replaces it with the subtraction function Data(+) – Data(-). Figure 5g uses infinite persistence to show applied jitter. Horizontal axis is 10 ns per division and vertical axis is 300 mV per division for all measured signals in all figures.

7 REFERENCES

1. Agilent Technologies, "Signal Integrity Solutions. Find Problems Now, Prevent Problems Next Time", 30th April 2010, Agilent Reference: 5988-5405EN.

2. Pete Scott, Steve Parkes, "SpaceWire Link Analyser Mk2: A New Analysis Device for SpaceWire Systems", International SpaceWire Conference 2010, St Petersburg, 22nd – 24th June 2010.

3. Steve Parkes, Martin Dunstan, "Debugging SpaceWire Devices using the Conformance Tester", International SpaceWire Conference 2007, Dundee, 17th – 19th June 2010.